Final Exam Summer

Course Name: Digital Logic Design

Submitted By:

Abdul Razzaq (12938)

BS (SE-8) Section: A

Submitted To:

Sir Amin

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Department of Computer Science,
IQRA National University, Peshawar Pakistan

Design/Digital Systems

Programs:

BS(CS)/BS(SE)/BS(TELC)

Course Codes: CSC-201/ SEC-201/TSC-201

EDP Codes: 102007016
Instructor: Muhammad Amin
Examination: Final Term
Semester: Summer 2020
Date: Sep. 26, 2020
Timing: 3:00 pm – 7:00 pm

Question No.	Q.1	Q.2	Q.3	Q.4	Q.5	Q.6	Q.7	Q.8	Q.9	
Total Marks	5	5	5	5	6	6	6	6	6	50

Note: Attempt all questions.

Q.1 Draw the logic circuit using the input (A, B, C, D) and output (X) waveforms in Figure 01.

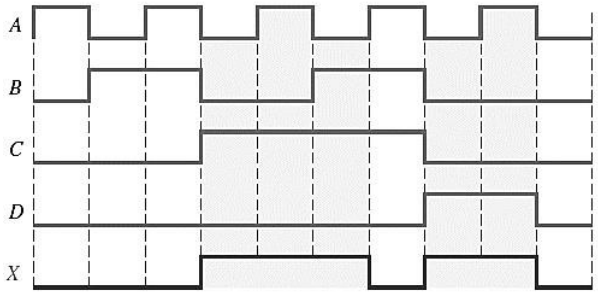
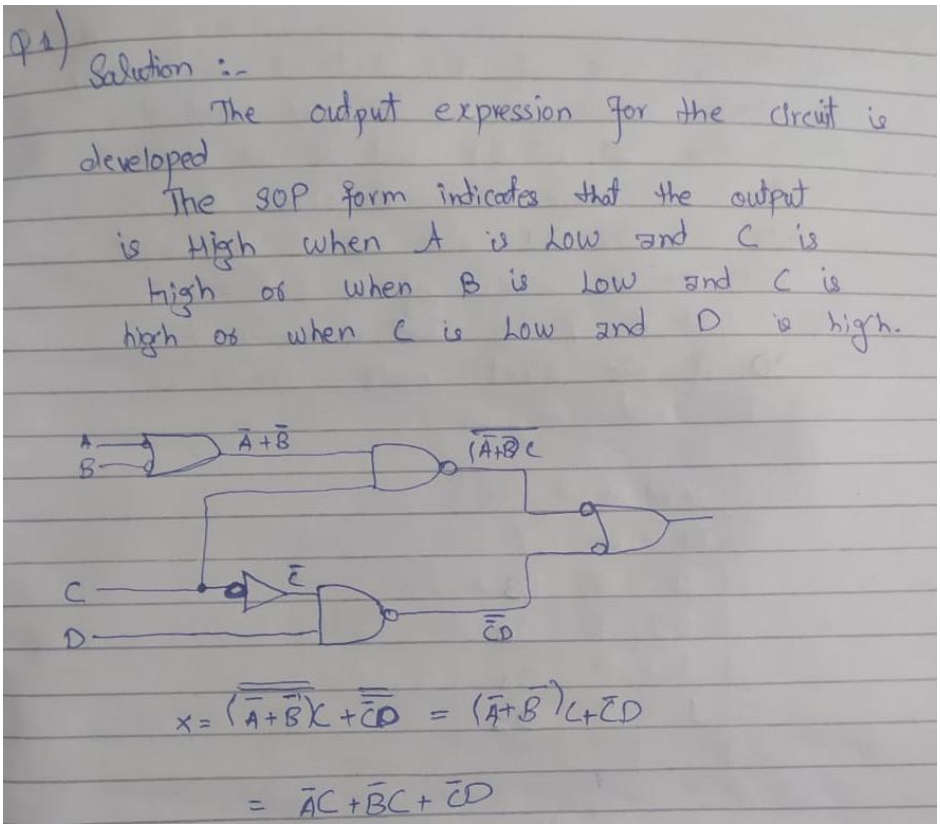


FIGURE 01

Answer:



Q.2 For the 4-input multiplexer, data inputs are given as:

$D_0 = 0$, $D_1 = 1$, $D_2 = 0$, $D_3 = 1$

Find the output Y if the select inputs are given as:

a) $S_0 = 1$, $S_1 = 0$

b) $S_0 = 0$, $S_1 = 1$

c) $S_0 = 1$, $S_1 = 1$ What is the output?

Q2)

The truth table of a 4-to-1 multiplexer is shown below in which four input combination 00, 10, 01 and 11 on the Select lines respectively switches the inputs D0, D2, D1 and D3 to the output.

That means when $S_1 = 0$, $S0 = 0$, the output at Y is D3, similarly Y is D0 if the select inputs $S_1 = 0$ and $S0 = 1$ and so on.

Select	Data input	output
S_1	S_0	Y
0	0	D3
0	1	D0
1	0	D1
1	1	D2

Q.3

For the circuit in Figure 02, assume the inputs are $\overline{Add}/Subt. = 1$, A = 1010, and B = 1101.

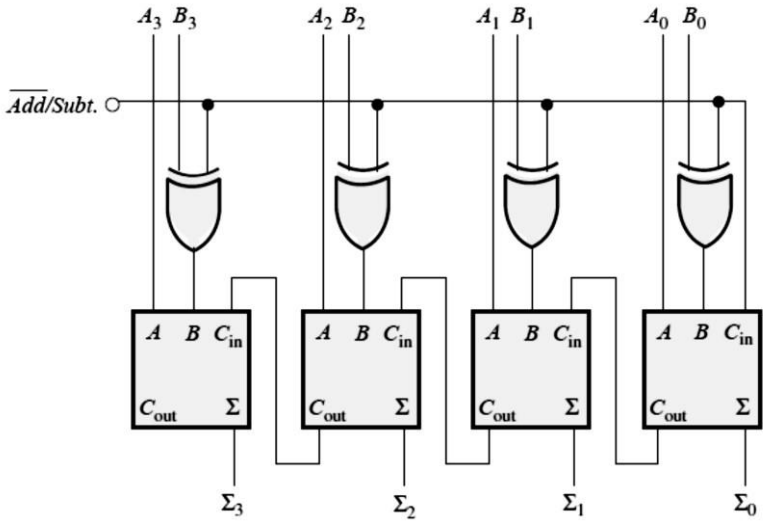
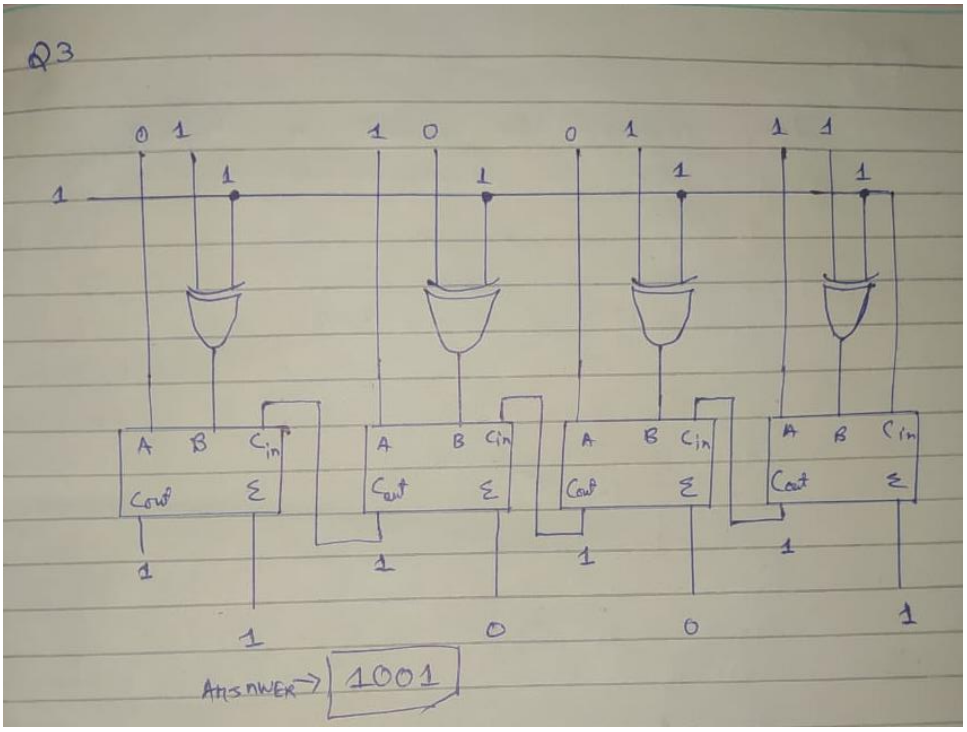


FIGURE 02

Answer:



Q.4 Determine the A = B, A > B, and A < B outputs for the input numbers shown on the comparator in Figure 03.

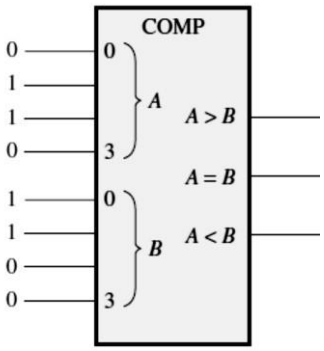


FIGURE 03

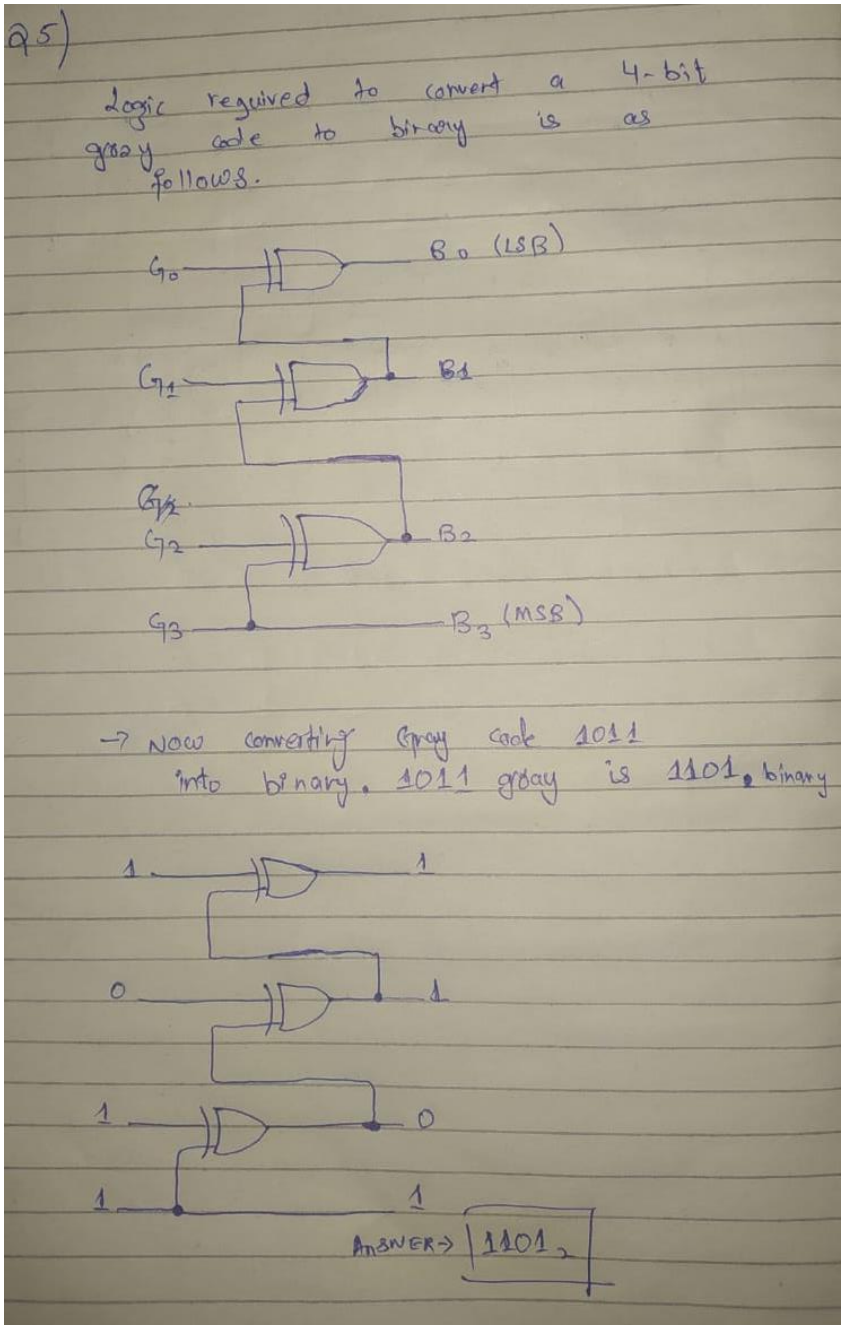
Answer:

The Number on the A inputs is 0110 and the number on the B inputs is 0011.

The A > B output is HIGH and the other outputs are LOW

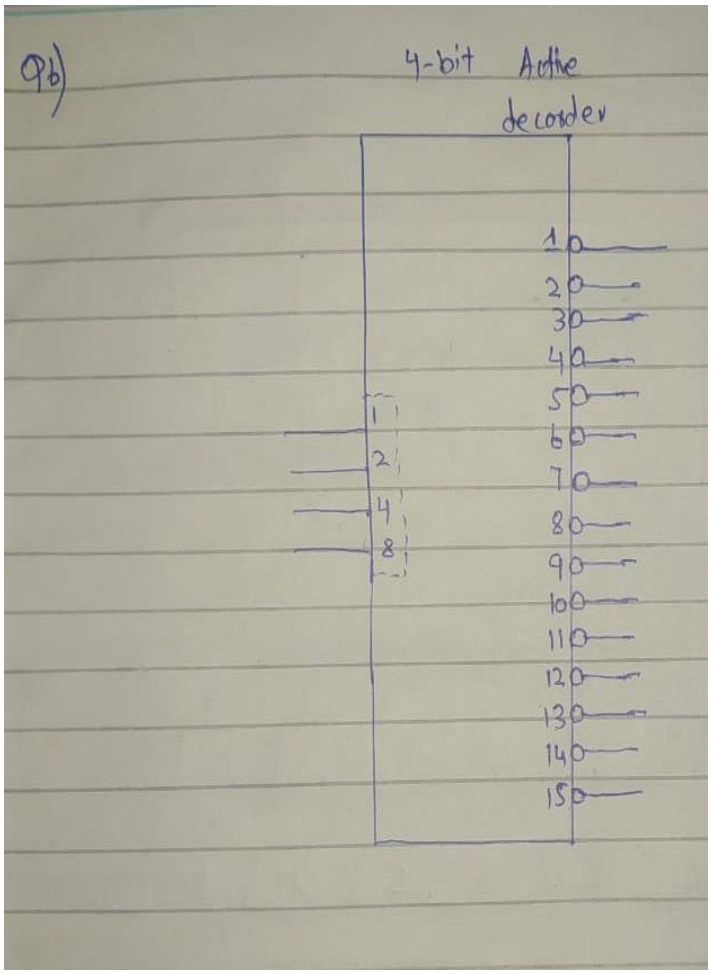
Q.5 Show the logic required to convert a 4-bit Gray code to binary and use that logic to convert the following Gray code words to binary: 1011

Answer:



Q.6 Draw and explain the logic diagram for 4-bit active low decoder.

Answer:



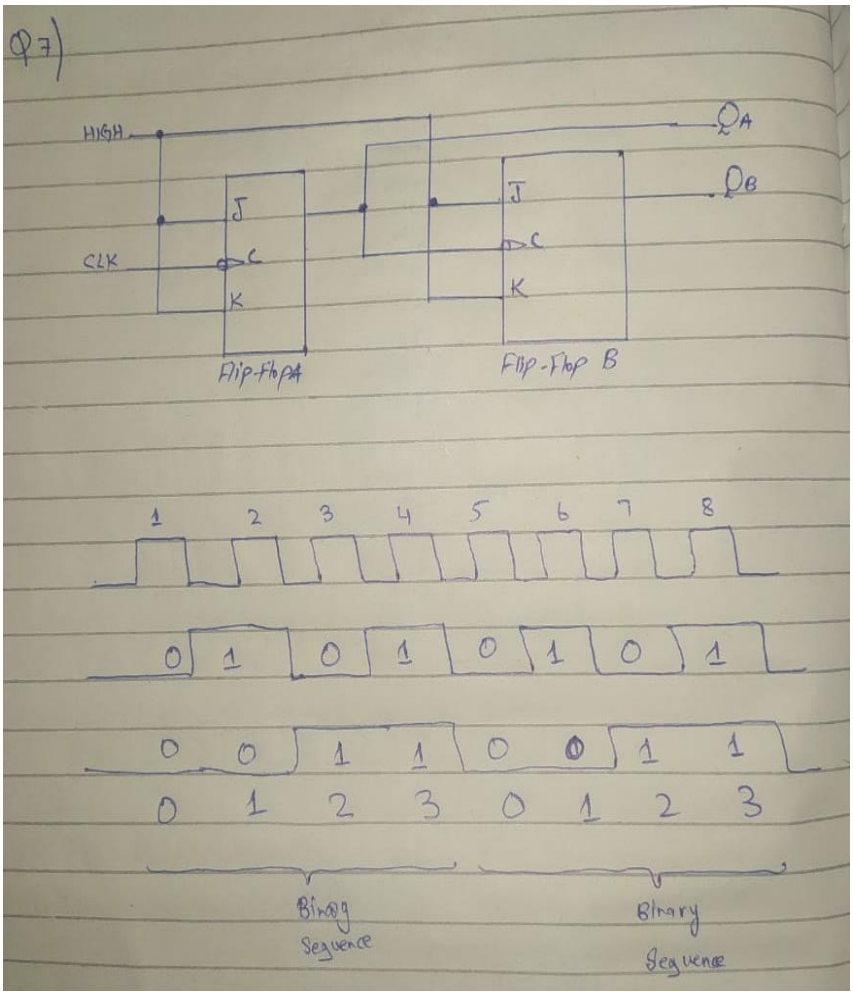
The 4-Bith Decoder in order to decode all possible combination of four bits, sixteen decoding gates are = 16). This type of decoder is commonly called either a 5-line to 16 line decoder because there are four inputs and sixteen outputs or a 1 of 16 decoder because for any given code on the inputs, one of the sixteen outputs is activated. A list of the sixteen binary codes are their corresponding decoding functions is given in the inputs, one the sixteen output is activated. A list of the sixteen binary codes and their corresponding decoding functions is given in diagram.

If an active-LOW out is required is required for each decoded number, the entire decoder can be implemented with NAND gate and inverters. In order to decode each of the sixteen binary code, sixteen NAND gates are required (AND gates can be used to produce active-HIGH outputs).

A logic symbol for a 4-line-to-16-line (1-16) decoder with active-LOW outputs is shown id diagram. The BIN/DEC label indicates that a binary input makes the corresponding decimal output active.

Q.7 Draw and explain the logic diagram for frequency divider (Use 3 J-K flip-flops and assume 16 kHz frequency of the initial wave-form.)

Answer:

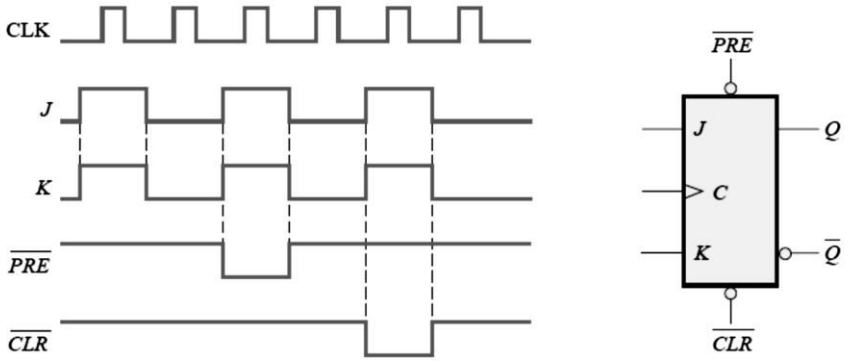


The logic diagram for frequency divider using 3 J-K flip-flop and assume 16 KHz frequency of the intimal wave-form the negative edge-triggered J-K flip-flop are used for illustration. Both flip-flop are initially RESET.

Flip-Flop a toggles on the negative-going transition of each clock pulse. The Q output of flip-flop. A clocks flip-flop B, so each time QA makes a HIGH-to-LOW transition, flip-flop B toggles.

The resulting QA and QB waveforms are shown in the diagram.

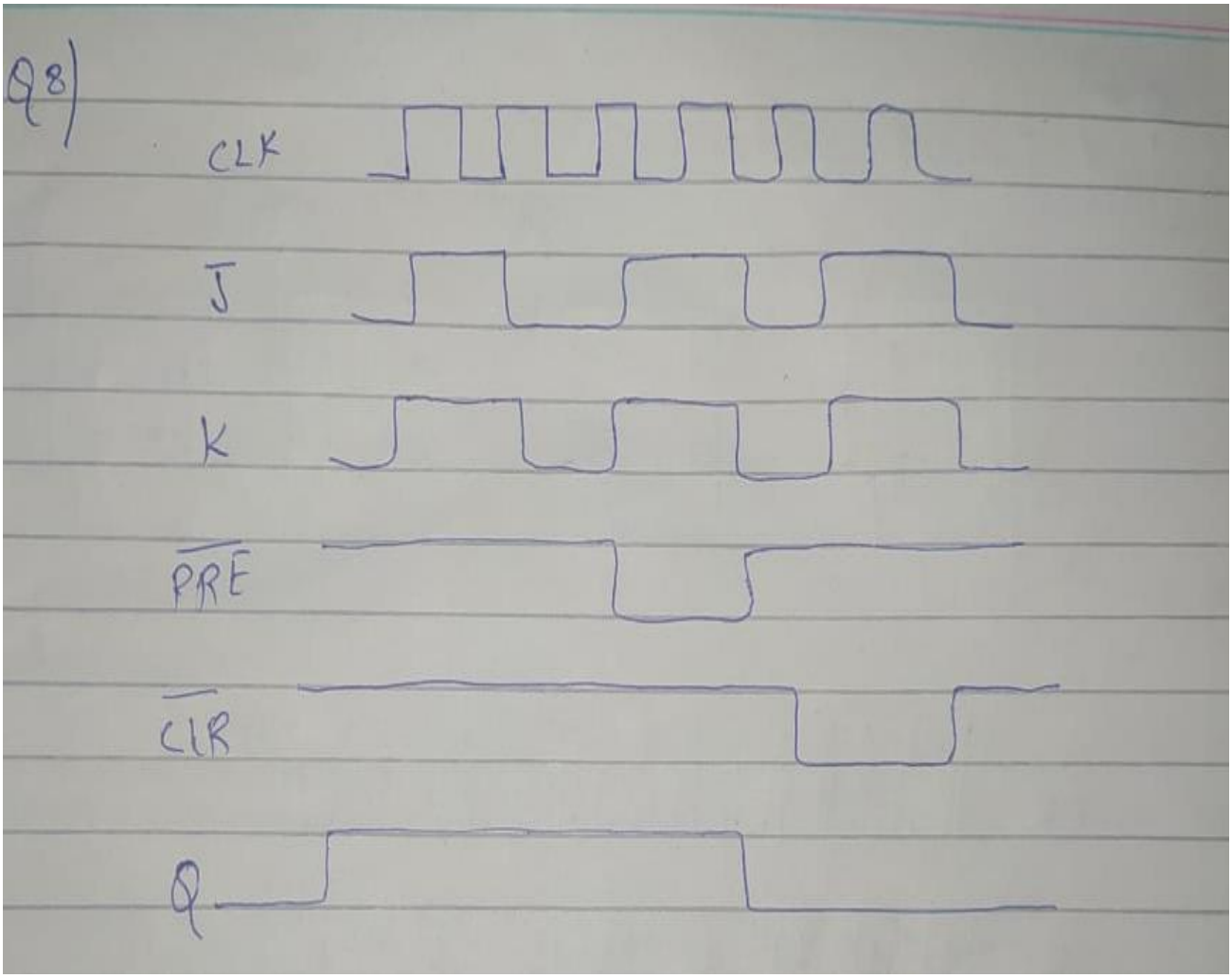
Q.8 Determine the Q waveform relative to the clock if the signals shown in Figure 04 are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW.



Q----------?

FIGURE 04

Answer:



Q.9 Draw the logic diagram and timing diagram for the 4-stage synchronous binary counter. Verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.

Answer: