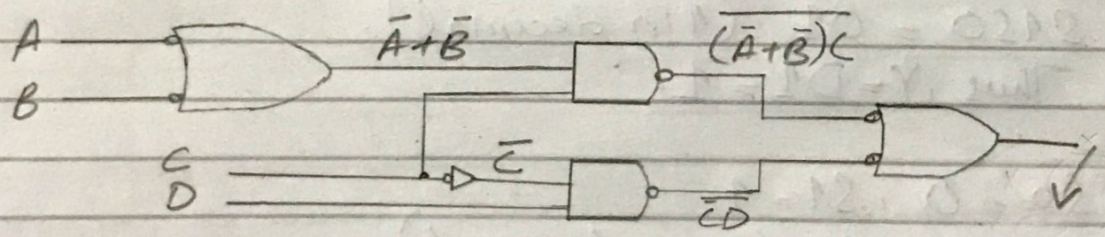
Q1 Draw the logic circuit using the input (A, B, C, D) & out put (x) waveforms in figure 01.

Ans Solution

The output expression for the circuit is develop in . The SOP from indecates that the output is HIGH when A is low & C is HIGH or when B is low & C is HIGH or when C is Low & D is HIGH.



$$X = \overline{(\bar{A}+\bar{B})C} + \overline{\bar{C}\bar{D}} = (A+B)C + \bar{C}D = \bar{A}C + \bar{B}C + \bar{C}D$$

Q2 For the 4-input multiplexer, data inputs are given as.

Ans

In multiplexer, the output Y takes the value of the input corresponding to the select bits. Select bits are S1S0.

Using this we can find the value of Y given the select inputs.

a|- S0 = 1, S1 = 0
S1S0 = 01 (1 in decimal).
Thus, Y = D1 = 1.

b|- S0 = 0, S1 = 1
S1S0 = 10 (2 in decimal)
Thus, Y = D2 = 0.

c|- S0 = 1, S1 = 1
S1S0 = 11 (3 in decimal).
Thus, Y = D3 = 1.

d). S0 = 0, S1 = 0.
S1S0 = 00 (0 in decimal).
Thus, Y = D0 = 0.

Q3 For the circuit in figure 02, assume the inputs are $\overline{Add/subt.} = 1$, A = 1010, & B = 1101.
What is the output?

Answer.

Let us say ADD/SUB as K.
If K = 1 it work as 4 bit subtractor.
If K = 0 it works as 4 bit adder.
we know A − B = A + B' so first find B' and then add.

Given

$\overline{Add/subt} = 1$

A = 1010 &
B = 1101

as adder & subtractor

If say K $\overline{Add/sub} = 0 \Rightarrow$ it work as adder
$\overline{Add/sub} = 1 \Rightarrow$ it work as subtractor

for add/sub = 1 > k

A_3	A_2	A_1	A_0
1	0	1	0
B_3	B_2	B_1	B_0
1	1	0	1

① for first full adder

$B \oplus k = B_0$

$\Rightarrow B_0 = 1 \oplus 1$
$= 0$
$A_0 = 0 \Rightarrow A_0 + B_0 + C_0 = 0 + 0 + 1$
$\Sigma_0 = 1$
$C_1 = 0$

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(2) for second full adder.

$B_1 \oplus K = B_1$ & $C_1 = 0$

$B_1 = 0 \oplus 1$
$= 1$

$E_1 = A_1 + B_1 + C_1 = 1 + 1 + 0.$
$C_2 = 1 \quad = 0.$

Simplify other two adders.

$A + \bar{B} = A - B$ (when $K = 1$)

$A = 1010.$

$B = 1101 \Rightarrow \bar{B} = 0010.$

$A + \bar{B} = 1'0100$
0010
1100

$E_0 = 0$
$E_1 = 0$
$E_2 = 1$ Cout $= 0.$
$E_3 = 1$

Q4 Determine the A=B, A>B & A>B & A<B outputs for the inputs numbers shown on the comparator in figure 3.

Answer

A comparator first compares the MBB (Most Significant Bit) to the two numbers A & B If the bit of A=1 & bit of B=0, then A>B. Similarly if the bit of A=0 & Bit of B=1, the A<B.

If Both have there MBs as 0 or 1, then the comparator Compares the next significant bit & so on till all the pairs of bits are compared.

Here A=0110 & B=0011.

First we compare the MSB (bit 3) of A & B.
Bit 3 of A=0 & Bit 3 of B=0.
As we both bits are 0, so we move to the next significant bits.
Now we Compare the Bit 2 of A & B.
Bit 2 of A=1 & Bit 2 of B=0.

So A>B, output is HIGH & other outputs are Low.

Q5 Show the Logic required to convert 4-bit Gary code to binary & use the Logic to convert the following Gray code words to binary: 1011.

Solution.

Gray Code to Binary.

$b_3 = g_3 = 1$

$b_2 = b_3 \oplus g_2 = 1 \oplus 0 = 1.$

$b_1 = b_2 \oplus g_1 = 1 \oplus 1 = 0.$

$b_0 = b_1 \oplus g_0 = 0 \oplus 1 = 1.$

∴ Binary: 1101.

Q6 Draw & explain the logic diagram for 4-bit active low decoder.

Ans The simple example below of a 2-to-4 line binary decoder consists of an array of four AND gates. The 2 binary inputs labelled A & B are decoded into one of 4 outputs, hence the description of 2-to-4 binary decoder. Each output represents one of the miniterms of the 2 input variables. (each output = a miniterm).

The binary inputs A & B determine which output line from Q0 to Q3 is "HIGH" at logic level "1" while the remaining outputs are held 'low' at logic "0" so only one output can be active (HIGH) at any one time. Therefore, whichever output lines is "HIGH". identifies the binary code present at the input, in other words it "de-codes" the binary input.

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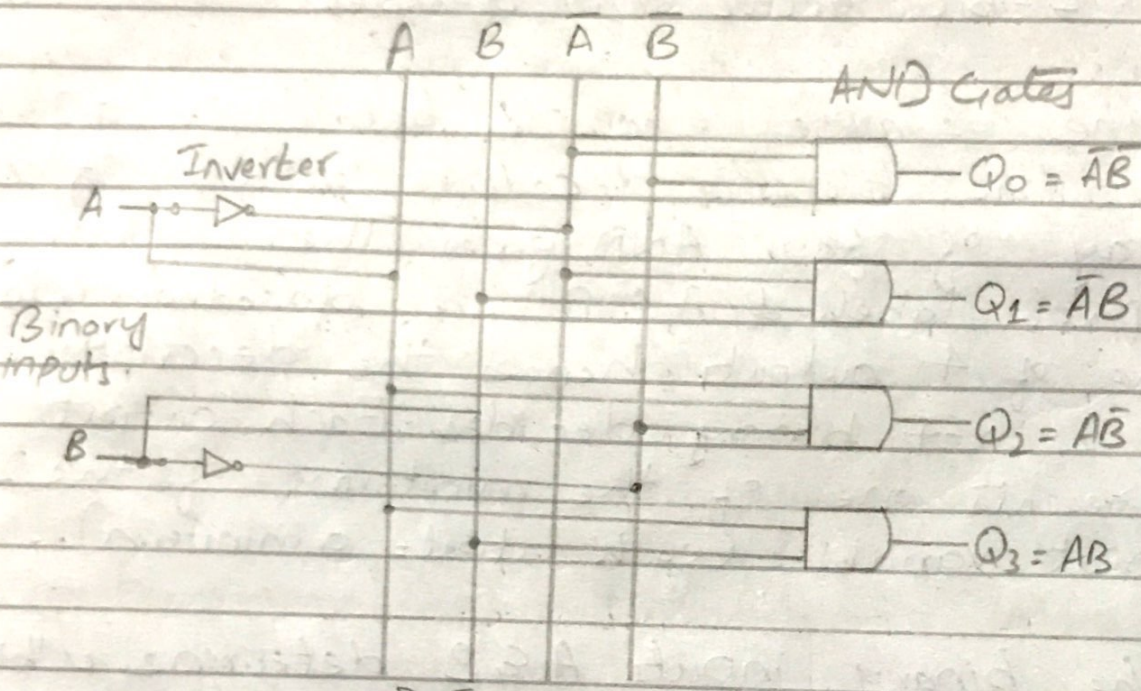
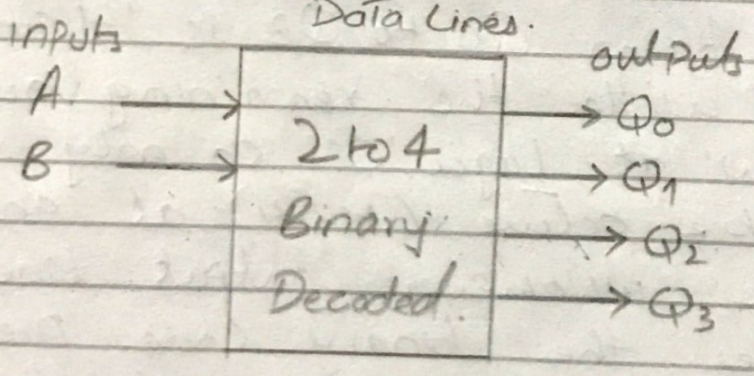
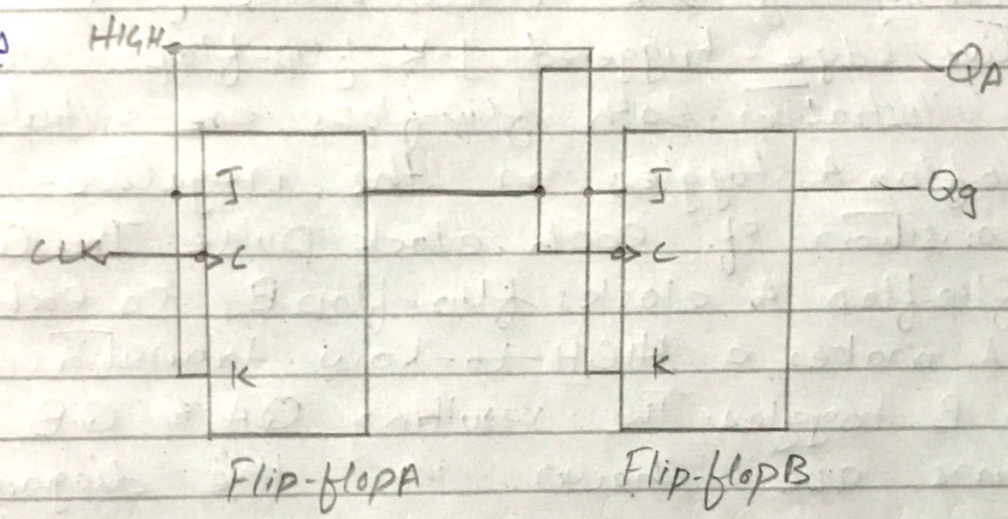
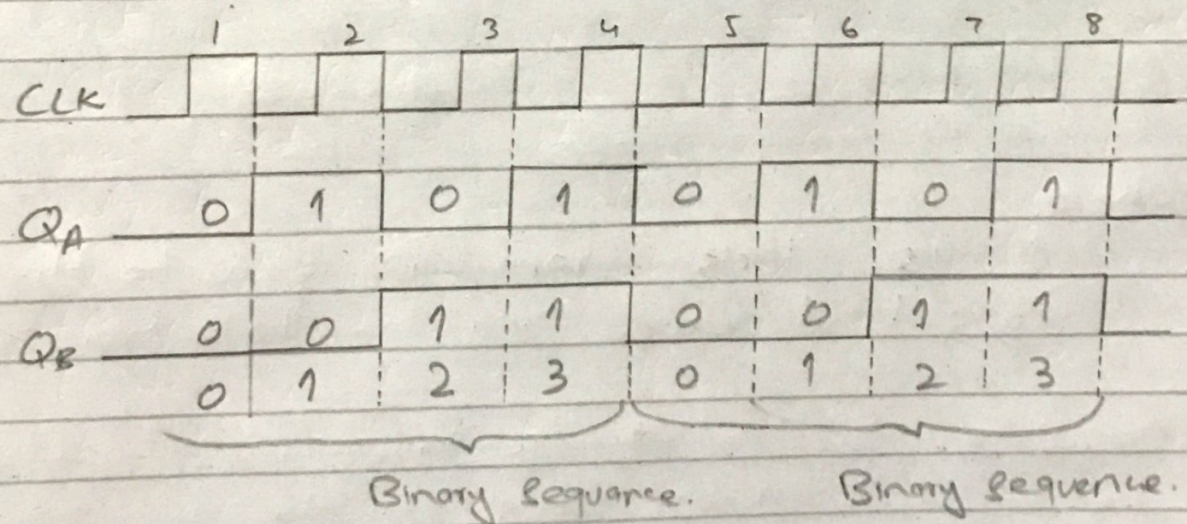




Q7 Draw & explain the logic diagram for frequency divider (use 3 J-K flip-flops and assume 16 KHz frequency of the initial wave-form).

Ans





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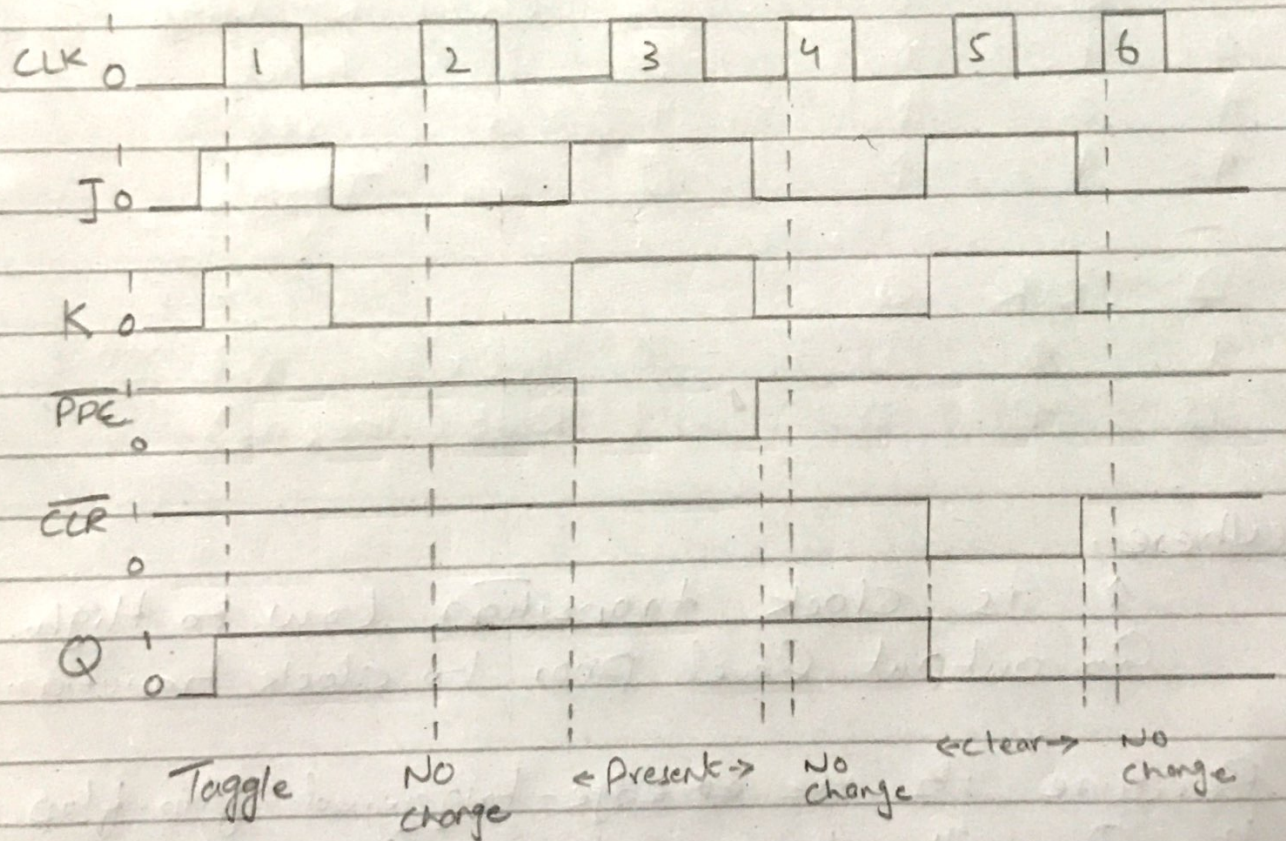
Explaination:

In logic diagram for frequency divider using 3 J-K flip-flops & assume 16 KHz frequency of the intial wave-form. the Negative edge-triggered J-K flip-flops are used for illustration. Both flip-flops are initially Reset. Flip-flop A toggles on the negative-going transition of each clock pulse. The Q output flip-flop A clocks flip-flop B, so each time QA makes a HIGH-to-Low transition, flip-flop B toggles. The resulting QA & QB wave forms are shown in the diagram.

Q8 Determine the Q wave form relative to the clock if the signals shown in figure 4 are applied to the inputs of the the J-K flip-flop. Assume that Q is initially Low.

Ans.



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Solution:

Truth table for +ve edge-triggered J-K flip flop:

Inputs			outputs		
J	K	CLK	Q	$\bar{Q}$	Comments.
0	0	↑	Q_0	$\bar{Q}_0$	No change.
0	1	↑	0	1	Reset
1	0	↑	1	0	Set
1	1	↑	$\bar{Q}_0$	Q_0	Toggle

D	CLK	Q		
1	↑	1	0	Set (stores a1)
0	↑	0	1	Reset (stores a_0).

Where,

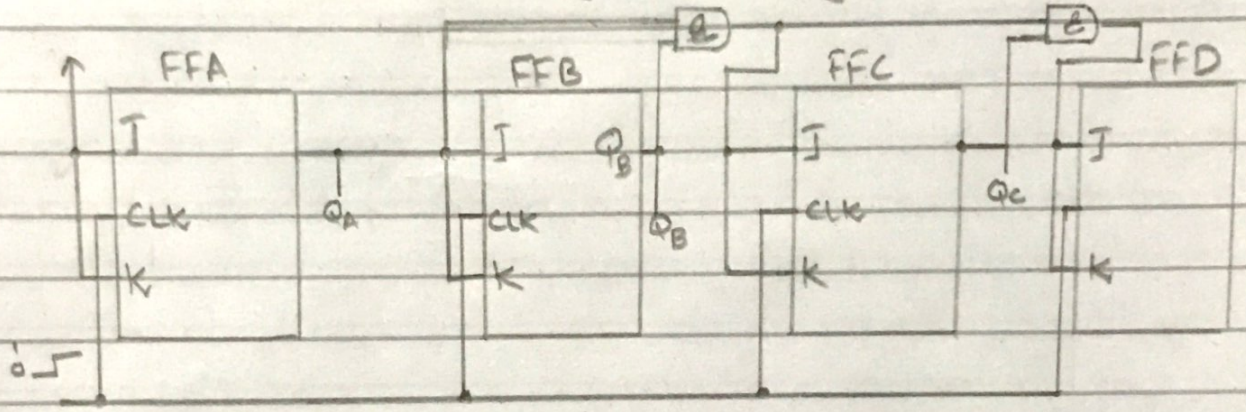
↑ is clock transition Low to High.
Q_0 output level prior to clock transition.

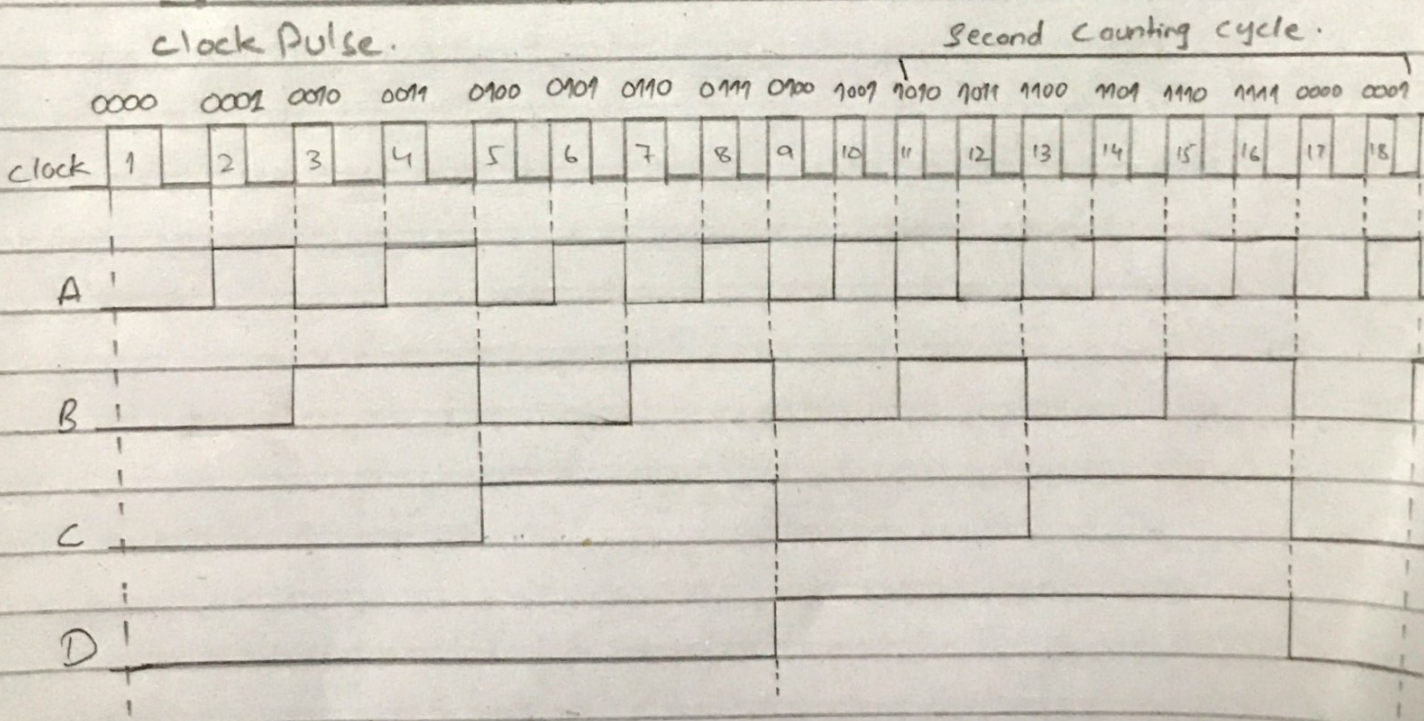
Because its +ve edge-triggered flip-flop, the Q will change only on the +ve-going edge of clock pulse.

Q9 Draw the logic diagram & timing diagram for the 4-stage synchronous binary counter. verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.

Ans

Binary 4-bit Synchronous Up counter.





In the above image, clock input cross flip-flops & the output timing diagram is shown. on each clock pulse, Synchronous counter counts sequentially. The counting output across four output pin is

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incremental from 0 to 15, in binary 0000 to 1111 for 4-bit synchronous up counter. After 15 or 1111, the counter reset to 0 or 0000 & count once again with a new counting cycle.