Assignment : No 2

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Questions No 1

Give Answer each of the following

Question No: 1(A)

Different desktop application that require that great power of Contemporary microprocessor based system are:

Image processing
Three dimensional rendering
Speech recognition
Videoconferencing
Multimedia authoring
Voice and video annotation of files
Simulation modeling

Questions No 1(B)

Answer

The techniques used in Contemporary processors to increase

Branch [illegible]
increases the amount of work available for the processor to execute.

* Superscalar execution

This is the ability to issue more than one instruction in every processor clock cycle. In effect multiple parallel are used.

* Data flow analysis

as busy as possible by executing instructions that they are likely to needed.

Question No 1(c)

* **Answer**

Discuss the prembleam created due to increases in clock speed and logic density of the processor are:-

* **Power**:-

As the density of the logic and the clock speed on a chip increases so the power density

increases and also dissipated the heat

* RC delay

The speed at which electrons can flow on a chip between transistors is limited by the resistance and capacitance of the metal wires connecting them:-

Specifically, delay increases as the RC product increases.

* @Memory latency:-

Memory access speed (latency) and transfer speed (through put) lag processor speeds.

Questions No 1(D)

* @Answer:-

The speedup using a parallel processor with N processors that fully exploits the parallel portion of the program

is as follows:

Speedup = Time to execute program on a single processor / time to execute program on N parallel processors

$$= T(1-f) + Tf/T(1-f) + Tf/N = 1/(1-f) + f/N$$

Questions No 1 (E)

* **Answer:**

* **Multicore:**

The use of multiple processors on the same chip provides the potential to increase performance without increasing the clock rate

* Strategy is to use two simpler

* processors on the chip rather than one more complex processor.

* With two processors larger caches are justified.

* As caches became larger it made peformance sense to creat two and then three levels of cache on a clip MIC:-

*

* Leep in peformancee as well as the challenges in developing software to expoit such a large number of cores.

* The multicore and MIC stragy involves and MIC stratagy homogeneous collection of general purpose processors on single chip.

GPUS

Core designed to perform parallel operations on graphics data. Traditionally

a plug in graphics card, it is used to encode and render 2D and 3D graphics as well as process video
used as vector processors for a variety of application that require repetitive Compitations

Questions No 2

Solve each of the following

2(a)

Answer

Effective CPI

CPI = (1*46000) + (2*33000) + (2*16000) + (2*9000)/100

CPI = 162000/100

CPI = 1620

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MIPS Rate

MIPS rate = 60 MHz / 1620 * 106

MIPS rate = 60 * 106 / 1620 * 106

MIPS rate = 60 / 1620

MIPS rate = 0.37

Execution Time

T = IC / (MIPS * 106)

T = 104000 / (0.037 * 106)

T = 104000 / 37 * 103

T = 2811 * 10-3

T = 2811 * 10-3

T = 2.811 Sec

Questions No 2 (B)

Answer

For Machine A:

CPI = (1*8 + 3*4 + 4*2 + 3*4)*10^6/(8+4+2+4)*10^6

CPI = 40*10^6/18*10^6

CPI = 2.22

MIPS rate = 200MHz / 2.22*10^6

MIPS rate = 200*10^6 / 2.22*10^6

MIPS rate = 90

T = Ic / MIPS * 10^6

T = 18*10^6 / 90*10^6

T = 0.2 Sec

For Machine B

$CPI = (1*10+2*8+4*2+3*4) * 106$

$(10+8+2+4) * 106$

$CPI = 46124$

$CPI = 1.92$

MIPS rate $= 200MHz / 1.92 * 106$

MIPS rate $= 200 * 106 / 1.92 * 106$

MIPS rate $= 104$

Pg

Questions No 2(c)

C(a)

Answer

The MIPS rate could be computed as the following

MIPS rate = IC/T* 106

IC = MIPS rate *T* 106

Now by Computing the ratio

Questions No: 2(C)

C(b)

Answer

Regarding to the VAX 11/780 the CPI (5MHz) 1(1*106/1*106

= 5/1 = 5

Regarding to the IBM RS/6000, the CPI = (25MHz) 1/(18*106) = 25*106/18*106

= 25/18 = 1.4

Questions No 2(D

@Answer

a - Determine the Average CPI

@Answer

Since we have the same instruction mix, that means the additional instruction for each task could be allocated appropriately between the instruction types. There for the following table be gotten

Arithmetic and logic	1	60%
Loadd store with cache hit	2	18%
Branch	4	12%
Memory reference with cache mix	12	10%

The average CPI = (1x0.6)+(2x0.18)+(4x0.12)+(12x0.1 = 2.64 Therefore, The CPI has been increased since the time for memory access is also increased

b. Determine the corresponding Maps rate

MIPS = 400/2.64 = 152 Thus

Corresponding drop in the MIPS rate

C. Calculate the speedup factor.
The speedup factor equals to the ratio of the execution times. The execution time is calculated as the following

$$T = IC1 (MIPS * 106)$$

For the 8 processor each processor execute 1/8 of the 2 million instructions plus the 25000

$$T8 = 2 * 106 \div 8 + 0.025 * 106 / 152 * 106$$

$$T8 = 18 \text{ ms}$$

Therefore we have

Speedup = Time to execute program

execute program on N parallel processor

Speedup = 11/18

Speedup = 6.11

Questions 2(D)(d)

By depending on the information given it is not obvious. How to quanty this effect in Amdahl's equation

Therefore if it is supposed that that fraction of code, which is parallelizable is f = 1, than Amdahl's law decreases to Speedup = N = 8

Therefore.

The actual speedup is only but 75% of the theoretical speedup