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Assignment no : ~~6th~~ 5th  
Submitted to : Sir Amin  
Subject : Computer Architecture  
Semester : 4th

①

Q = Give detail answer to each of the following.

(a) Discuss different types of Semi-conductor memories in detail.

There are various types of Semi-conductor memories. The most common is referred to as RAM (random access memory). Most type have the property of random access memory which means that it takes the same amount of time to access any memory location.

\* Here is a table of Semi-conductor memory types.

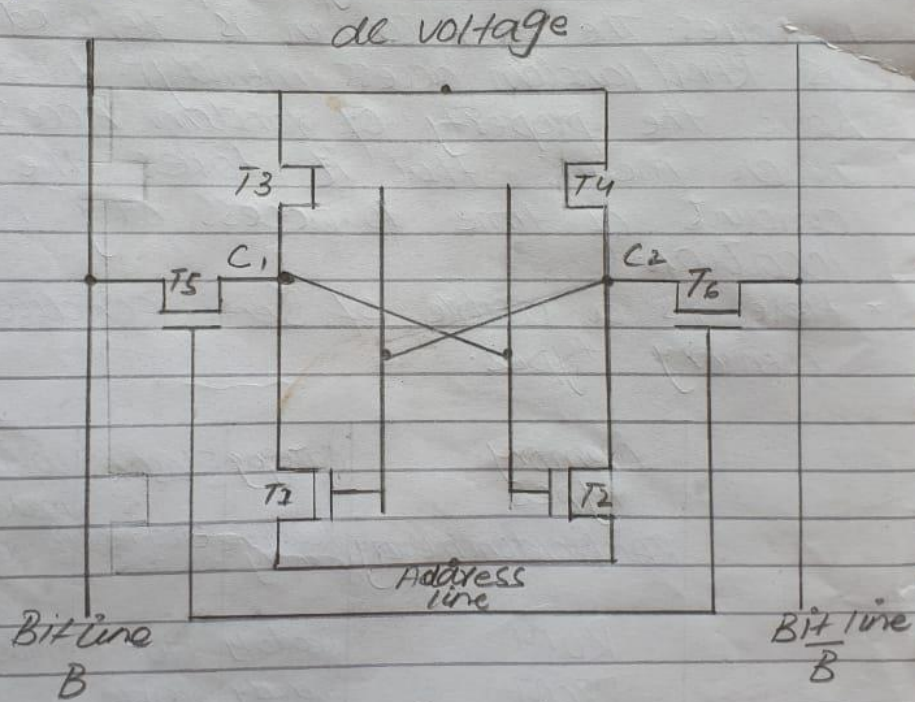
Memory types	Category	Erasure	Write mechanism	Volatality
RAM (random memory)	Read/write memory	Electrically Byte level	Electrically	Volatile
ROM	Readonly memory	NOT	MASKS	
PROM		Possible with chip level		
EPROM		Electrically Byte level		
EEPROM	Read most memory	Electrically block level	Electrically	Non volatile
Flash memory				

(b) Explain the read & write operation for the SRAM Cell using diagram.

\* Read operation

(2)

In SRAM for any operation to be performed the word line should be high. To perform read operation initially  
\* Write operation:-  
Consider the memory bits consist of  $Q=0$  &  $\bar{Q}=1$



(b) Static ram (SRAM) cell

(3)

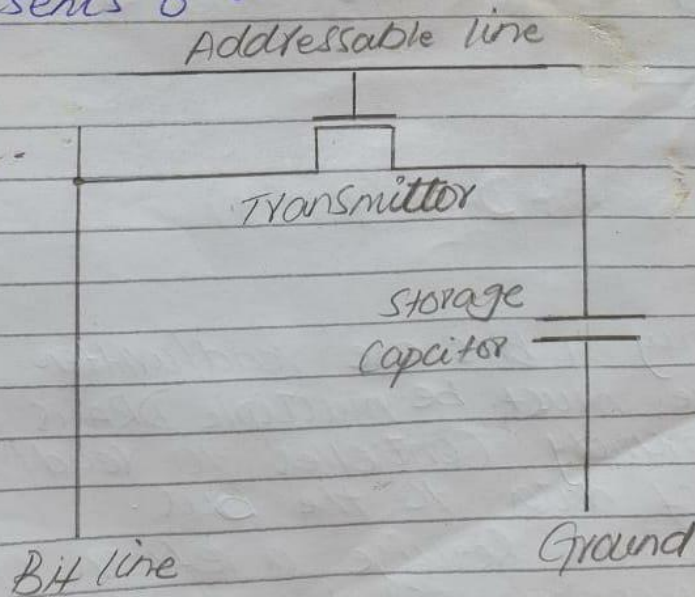
(C) Explain the read & write operation for the DRAM cell using diagram

Read operation:-

When the address line is selected the transistor turns on & the charge stored on the capacitor is fed out onto a bit line & to a sense amplifier. It compares the capacitor voltage to a reference value & determines if the cell contains a logic 1 or a logic 0.

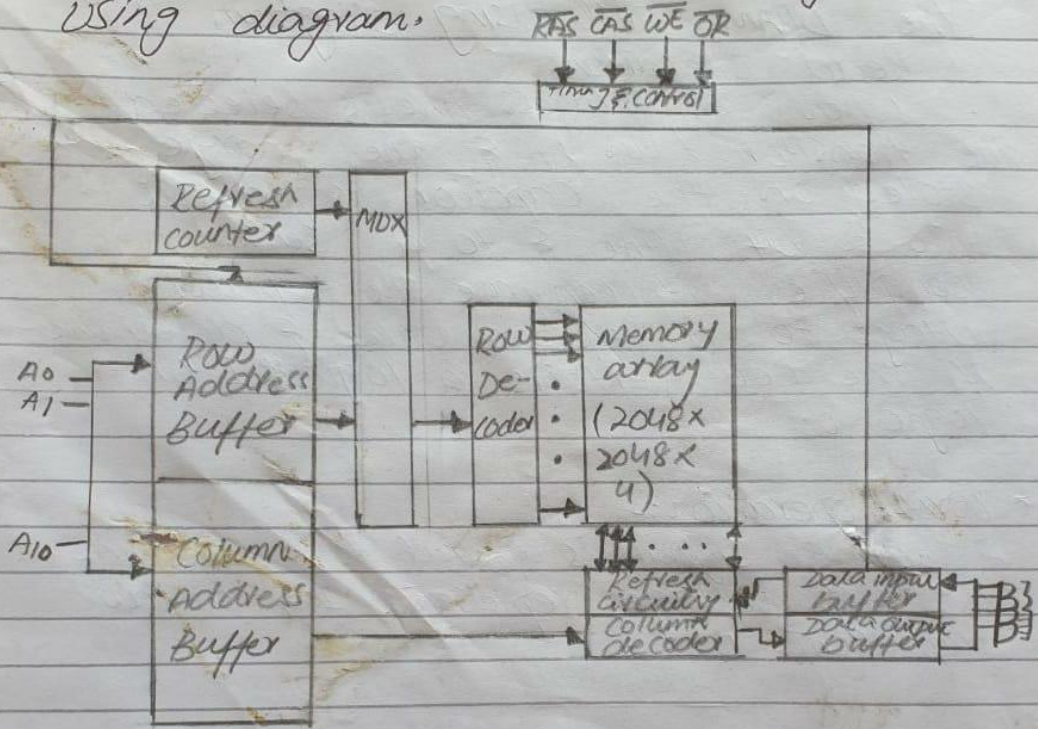
\* Write operation:-

A voltage signal is applied to a bit line, a high voltage represents 1 & a low voltage represents 0.



(4)

(d) Discuss 16-Mbit DRAM (4Mx4) organization using diagram.



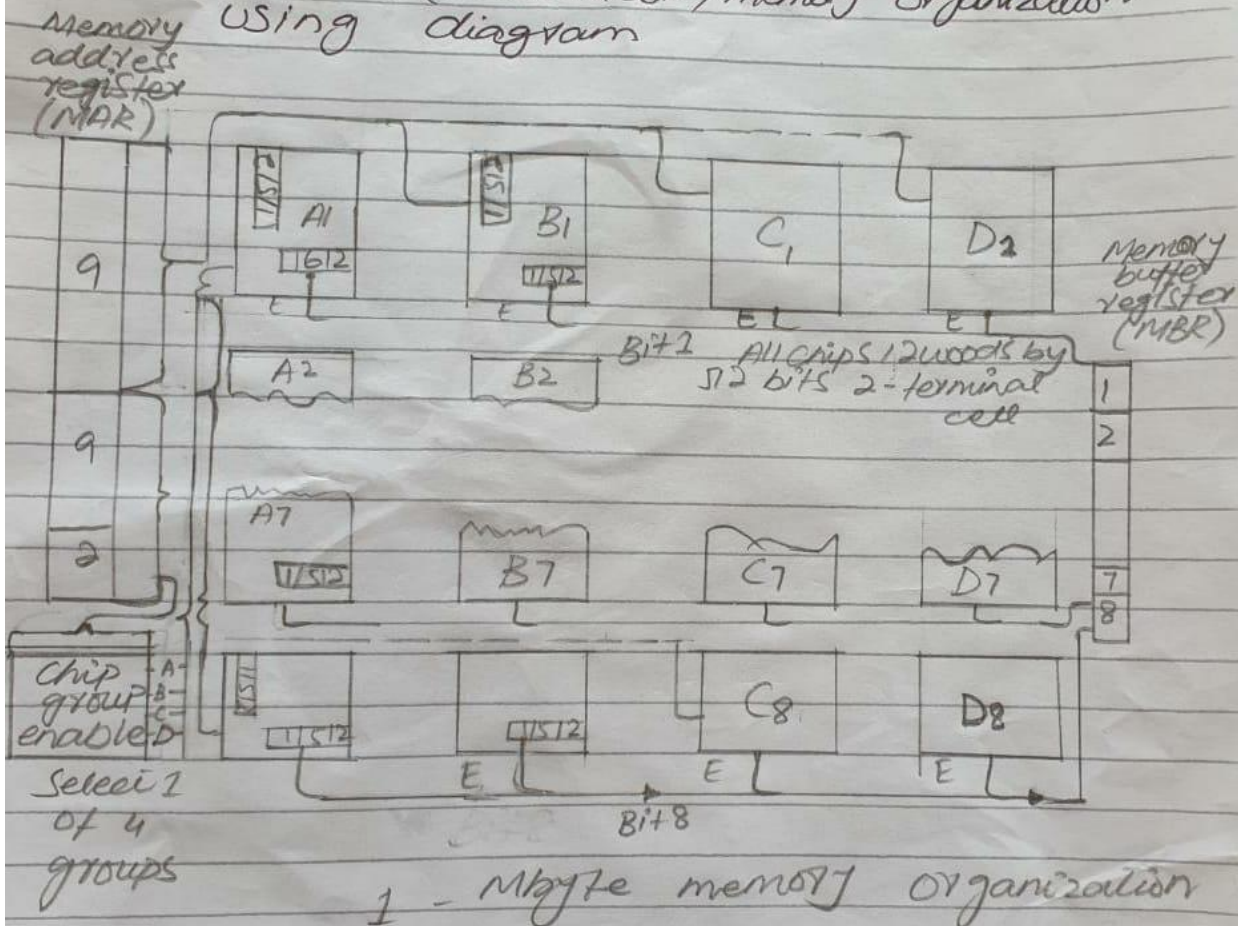
Typical Megabit DRAM (4Mx4)

Because only 4 bits are read/written to their DRAM, there must be multiple DRAMs connected to the memory controller to read/written a word of data to the bus.

All the DRAMs require a refresh operation. A simple technique for refreshing is in effect to disable the DRAM chip while all data

(5)

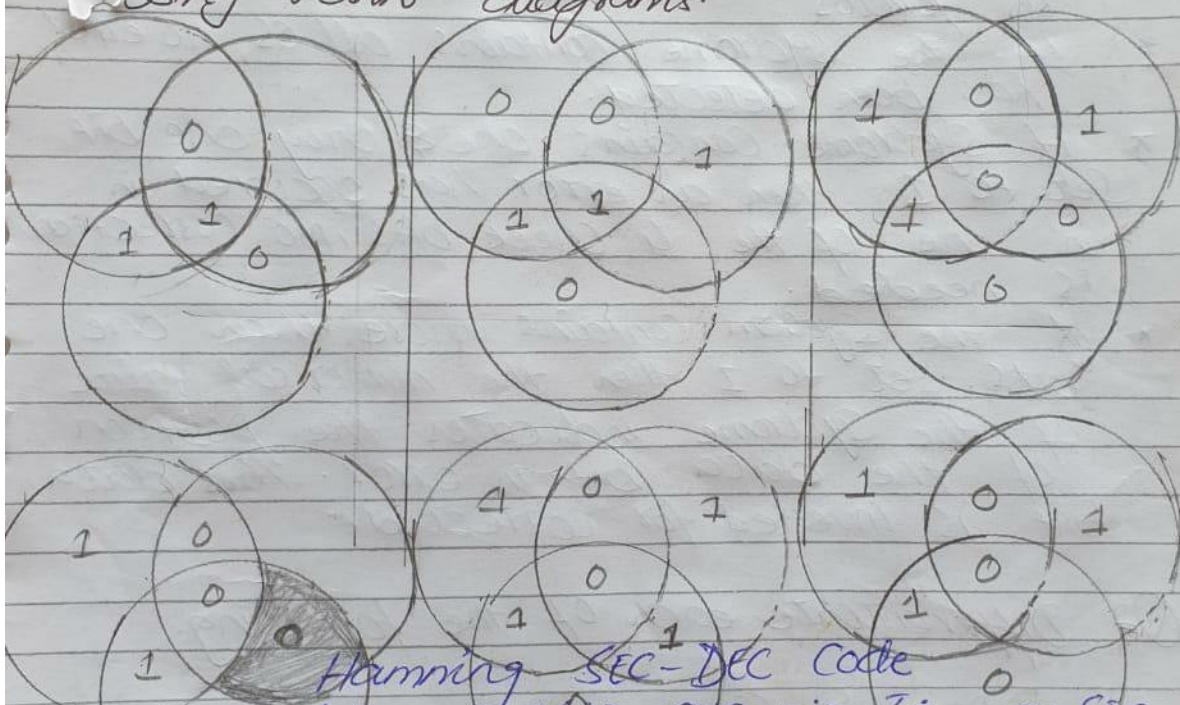
Cells are refreshed. The refresh counter steps through all of the row values. This causes each cell in row to be refresh  
c) Discuss 1MB (256K x 4 x 8Bit) memory organization using diagram



(6)

The possible organization is secured of a memory consisting of 1M word by 8 bits per word. In this case we have four columns of chips, each column containing 256K words arranged.

(f) Explain Hamming SEC-DEC code using venn diagrams.



Hamming SEC-DEC code with 0.1 bit per chip organization an SEC-DEC code is generally considered adequate e.g the IBM 30xx implementations used an 8 bits SEC-DEC code for each 64 bits of data in main memory. The size of main memory is actually about 12% larger than is apparent to the user

(7)

The Vax computers used a 7bits SEC-DEC for each 32 bits of memory for a 22% overhead.

g) How is Syndrome for the hamming code interpreted?

Syndrome for the hamming code interpreted as follows

- \* If the Syndrome contains all 0s, no error has been detected.
- \* If Syndrome contains one & only one bit set to 1 then an error has occurred in one of the 4 check bits, No correction is needed.
- \* If the Syndrome contains more than one bits set to 1 then the numerical value of the Syndrome indicates the position of the data bit in error. This data bit is inverted for correction.

Q2 Differentiate each of the following.

a) DRAM & SRAM

DRAM	SRAM
* DRAM is more dense & less expensive	* SRAM is expensive
* DRAM require the supporting refresh circuitry	* SRAM doesn't require any refresh circuitry.
	* SRAM are faster in speed than DRAM



(8)

- |  |   |
|--|---|
| <ul style="list-style-type: none"><li>* DRAM are normal in speed</li><li>* SRAM is used for cache memory</li></ul> | <ul style="list-style-type: none"><li>* DRAM is used for main memory.</li></ul> |
|--|---|

b) EEPROM & flash memory.

EEPROM	Flash memory
<ul style="list-style-type: none"><li>* EEPROM devices can erase any byte of memory at any time.</li><li>* EEPROM uses NOR type memory</li><li>* EEPROM is byte-wise erasable</li></ul>	<ul style="list-style-type: none"><li>* Flash memory can only erase an entire chunk or "sector" of memory at a time.</li><li>* Flash memory uses NAND type memory</li><li>* Flash is block-wise erasable.</li></ul>

Q NO # 3

$$M = 8$$

$$2^k - 1 > = k + m$$

$$2^4 - 1 > = 4 + 8$$

$$15 > = 12$$

1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	1	1	0	0	1	0	0	1	0

- \* The check bits are in bit numbers 1, 2, 4 & 8
  - \* Check bit 8 calculated by values in bit numbers: 9, 10, 11 & 12.
  - \* Check bit 4 calculated by values in bit numbers: 5, 6, 7 & 12
  - \* Check bit 2 calculated by values in bit numbers: 3, 6, 7, 10 & 11
  - \* Check bit 1 calculated by values in bit numbers: 3, 5, 7, 9, 10 & 11
- Thus the check bits are: 1011