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I'D 6966

Programm . B.Tech Electoral

Paper . Microprocessor

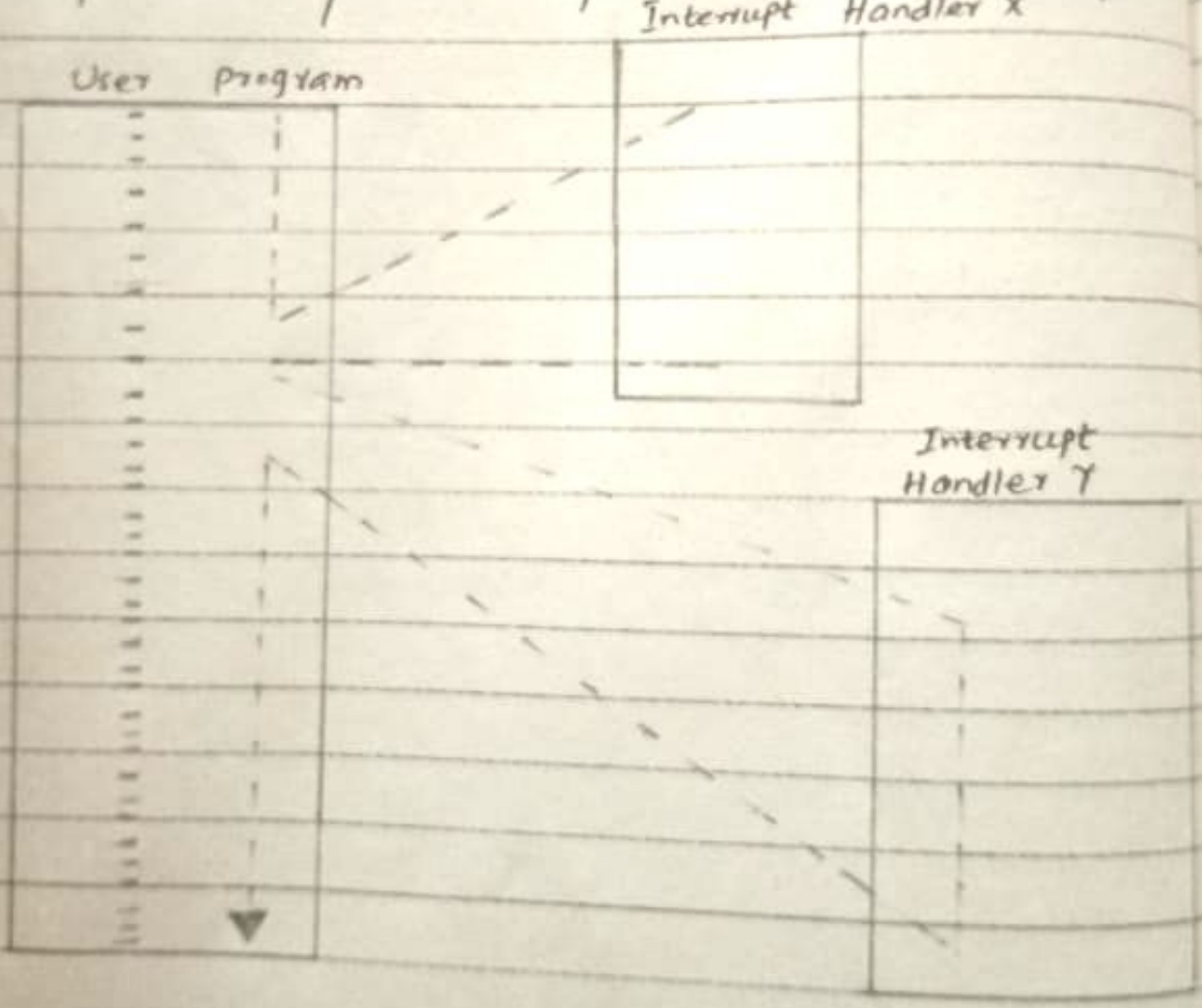
Submitted to Eng. Aamir Aman.

P # 1 ID. 6966

Q#1 (A) Explain the process of sequential and priority handling of interrupts.

Ans:

SEQUENTIAL & PRIORITY HANDLING OF INTERRUPTS:



Interupt Y comes after X → sequential service

P - To

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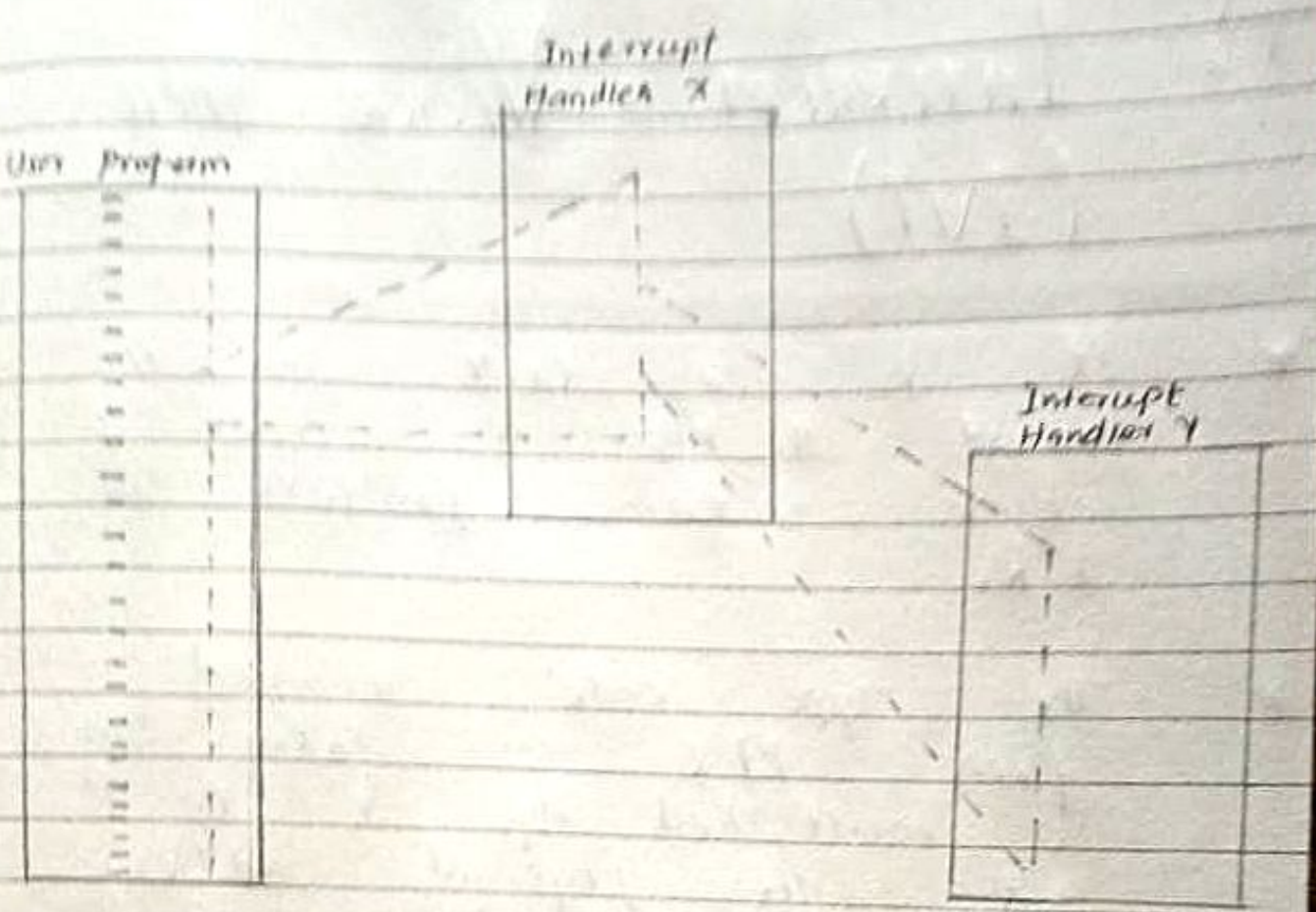

The sequential Multiple interrupts works by handing the interrupts in a strict sequential order. An interrupt is a signal From a device which causes a main program which is operating a computer to stop and figure out what is must do next:

Q1b) What dou you know about the interrupt vector Table (IVT)?

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Ans // INTERRUPT VECTOR TABLE (IVT)

* It is a table in the lowest 1 kB of memory which contain pointers to ISRs

* The Type code recieved from PIC on data bus is multiplied by 4 to get the physical address from where it search for the pointer of ISR in this table for the device which had sent the interrupt request to CPU.

P-T-O

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Interrupt type code	Description	Pointer Address	point to
00	Divide by zero	00000	7845:00CE
04	OverFlow	00010	0070:0756
05	Print screen	00014	F000:FF54
08	Clock Tick	00020	23E2:0174
09	keyboard action	00024	2C3A:14BA
0B	COM 2	002C	F000:210D
0C	COM 1	0030	F000:210D
0E	Floppy Disk A	0038	9106:0439
0F	LPT1 Printer	003C	0070:0756
19	Bootstrap startup Routine	0064	007D:18ED

Q.02 Question = (02) Part (A)

Ans Techniques to Overcome Problem.

Techniques to overcome the problem by these keys.

(1) **Two key lock out.**

During the second Scan if still two keys of a row are found depressed both keys will be locked out & neighter is accepted by the up.

(*) However if any one of them is released after first Scan, the second key still depressed will be accepted by up.

(6)

N key roll Over

The N+key during the second scan if still more than one key is found depressed, they are accepted by the NP.

The key entries are accepted in the order in which they were pressed.

(A)

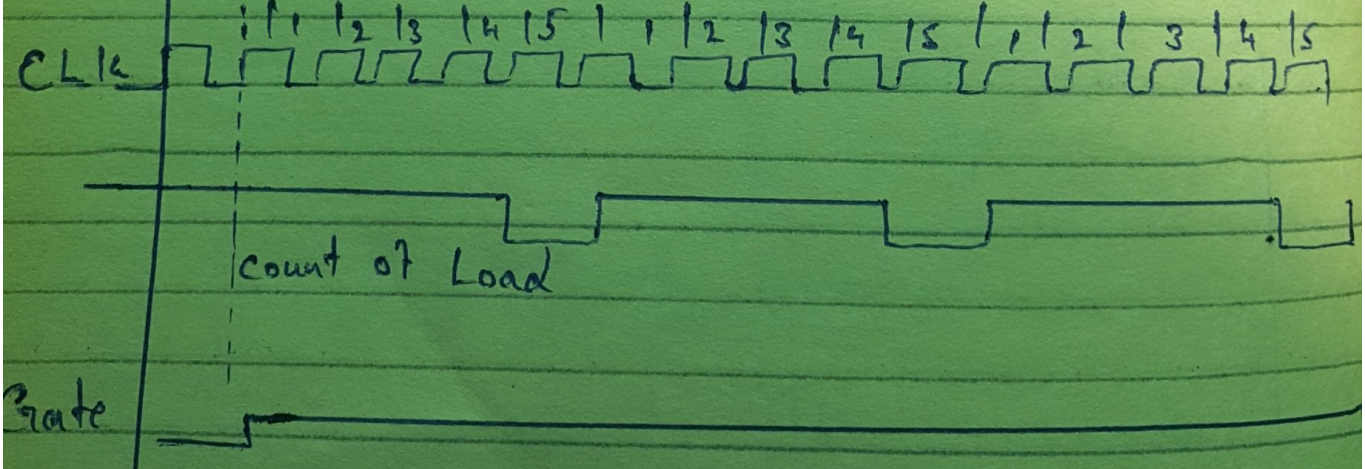
Question #(02) Part (B)

Ans 7

Rate Generator (mode)

The Rate generator mode a (initial value N=5)

(*) it divides the input clock frequency by N. when the counting starts, output become high. After 4 pulses, the out-put goes low for 1 clock period So for N clock cycles, 1 out put cycle is generated. Gate must remain high during counting.



Question :(03)
Answer :(03) Part (A)

DMA Process

DMA means a direct memory access. a dma is a featured of computer system, that allow certain Hardware subsystems to access main system memory (Random access memory)

DMA is also used for intra-chip data transfer in multi-core processor.

DMA sends DMAC request for data transfer.
DMAC sends high on Hold input C.P.U.
DMA controll C.P.U programm.
- CPU tells DMA controller
- I/O device address
- Amount of data transfer. Stating address of main memory.
CPU sends HLDA to DMAC & release the controll system bus.
DMA deals with transfer.
when done, the device sends low on DREQ pin to DMAC.
DMAC send low on HOLD Pin, telling CPU to controll System Bus.

Q(03) Part (B)

Q 03
Part=B
Ans
Ans 2

Ther Protocols for serial dat transfer can be grouped into two types.

Asynchronous	Synchronous
Data transfer there is no common clock signal b/w the sender and receiver.	The dat transfer both the sender and receiver access the data according to the same clock.
* special signals along the transmission medium.	Synchronous transmission by an external clock.
* Commonly used one to one communication	Used for short distance high volume in blocks (instead of individual characters) and fast tra
* There are many variants the simplest uses Just two lines Tx (transmit) / Rx (receive).	Synchronous serial communication interface I2C, SPI, Microwire, USB, IEEE 1394 (Firewire).
* it goes low for 1 bit (0.104)ms.	
* send out data LSB first (for 8 bits).	

Question :- (04) Part (A)

Ans :-

Status Signal :-

A status signal a busy signal or ready signal.

(*) a status signal which determine whether the address for input - output port or memory when it is high (1) the address on bus is for input - output device whe it is low (0) the address on the address bus to the memory So, S1. These are status signal.

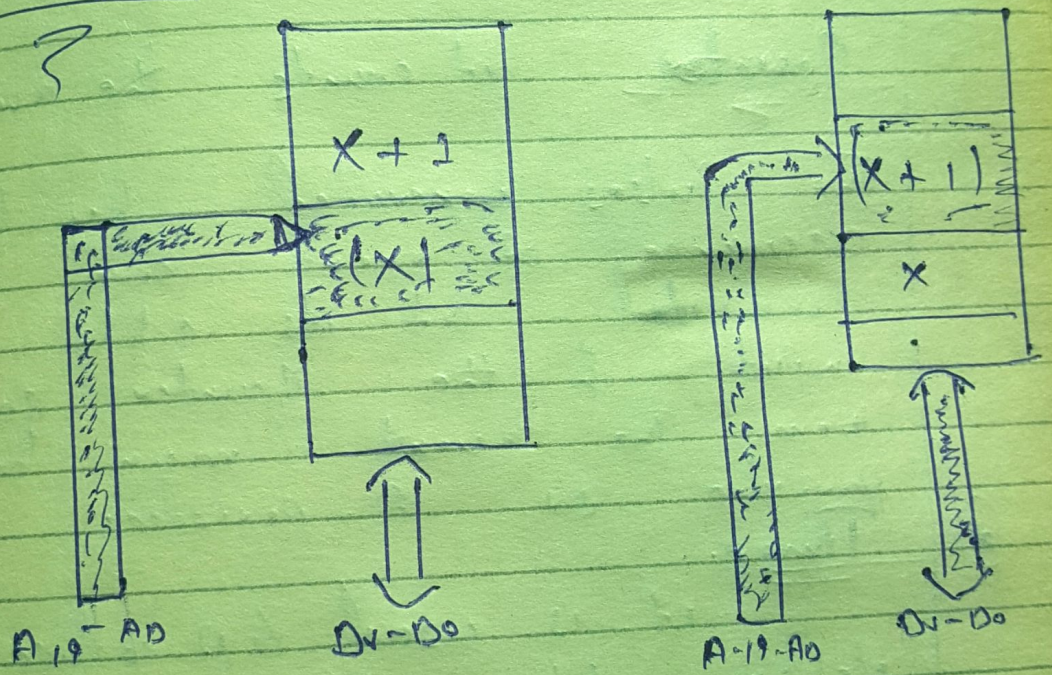
(*) 8085 µm has got three status signal So, S1, ~~four~~ and IO/ and a special signal ALE. its a read control sign when the signal on this pin is low selected memory input output device is red and information placed on data bus -

Question (4) Part (B)

Answer:

A word is transferred by 8088 microprocessor and interfacing.

Example:



Question. (05)
Part (A)

Ans 5

Counter & Timer.

8254 is an IC used as a counter or timer.

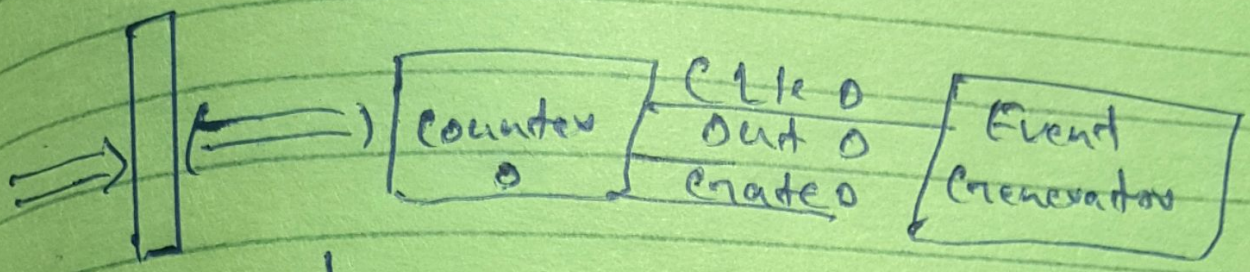
(1) **Counter** it counts the events.

The Pulses generated by the occurance of event are connected at its clk input & the counter counts them The event may be periodic or A-periodic.

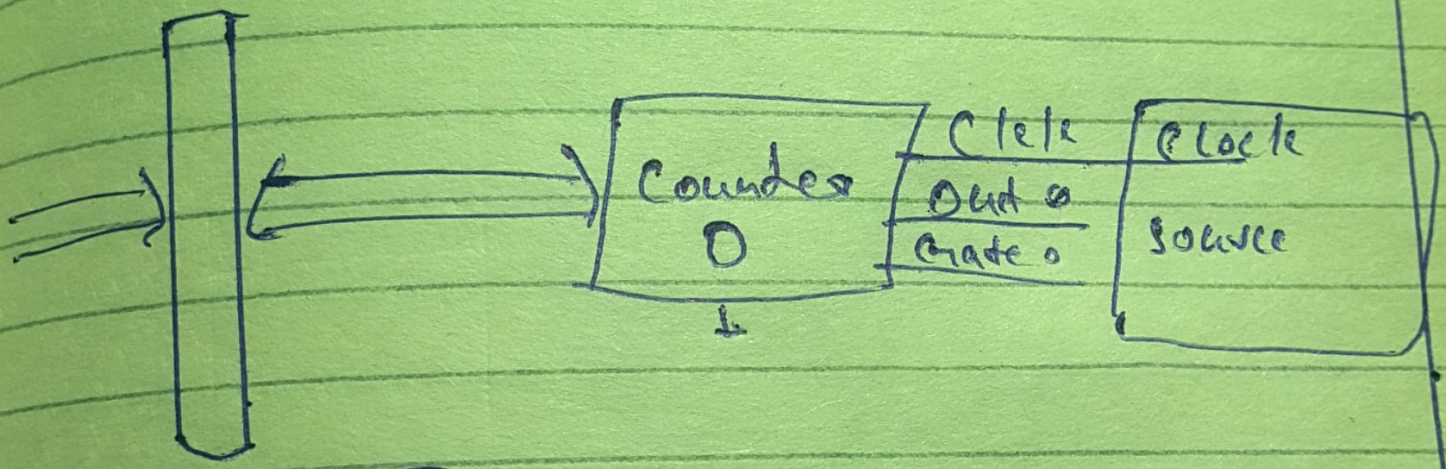
(2) **Timer.** it is used to produce delay blw two events.

The Pulses generated by the periodic Clock source are connected at its clk & the timer counts them.

Counter / timer.



Counter.



Timer.

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Q5) Explain with the help of hand diagram that how hand shaking is done in RS-232 interface?

Ans) The RS232 handshake process involves four steps:

1) The data terminal equipment (DTE) puts the RTS line into the "On" state.

2) The data communications equipment (DCE) puts the CTS line into the "On" state.

3) The DTE puts the DTR line into the "On" state.

4) The DTR line remains in the "On" state while data is being transmitted.

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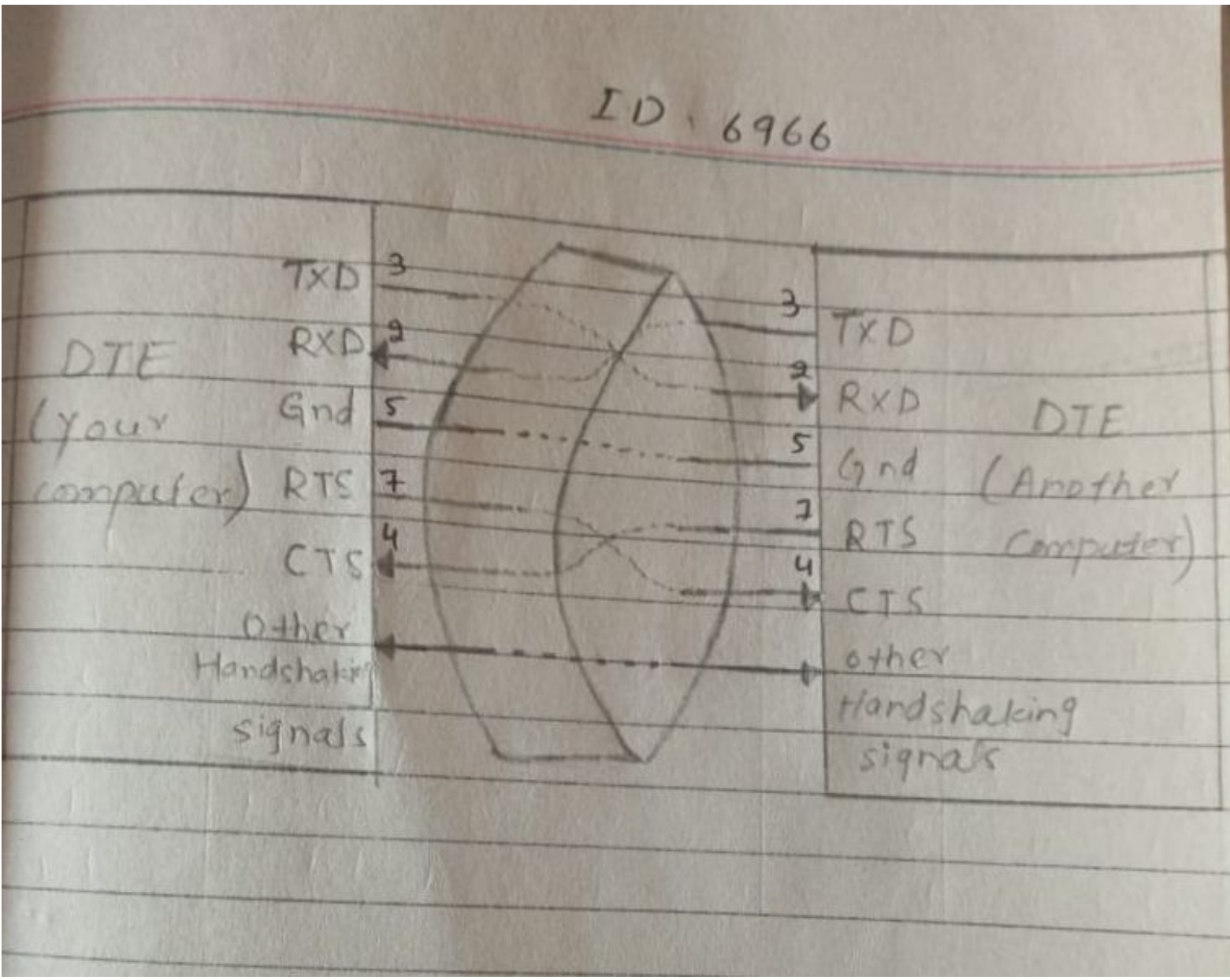
DTE
(your computer)
TXD
RXD
Gnd
RTS
CTS
Other Handshaking signals
3
2
5
7
4
3
2
5
7
4
TXD
RXD
Gnd
RTS
CTS
other Handshaking signals
DTE
(Another Computer)