1

(Q:NO: 1 Part a)

Addressable units:: In some system the addressable unit is the word. However, many systems allow addressing at the byte level. In any case, 2A = N.

Unit of Transfer. For main memory this is the number of bits read out of or written into memory at a time. The unit of transfer not equal a word or an adressable unit.

Word :; The natural unit of organization of memory. The size of a word is typically equal to the number of bits used to represent an integer and the to the instruction length.

(Q:NO:1 Par b)

Probably the most effective is least recently used (LRU). Replace that block in the set that has been in the cache longest with no reference to it. For two way set associative this is easily implemented. Each line include a USE bit when a line is referenced, its USE bit is set to 1 and the USE bit of the other line that set is set to 0. USE bit of the other line in that set is set to 0 when a block is to be read into the set, the line whose USE bit is 0 is used. Because we are assuming that more recently used memory location are more likely to be referenced. LRU should give the best hit ratio. LRU is also relatively easy to implement for a fully associative cache.

The cache mechanism maintains a separate list of indexes to all the lines in the cache. when a line is referenced it moves to the front of the list. for replacement the line at the back of the list is used Because of its Simplicity of use of implementation, LRU is the most popular replacement algorithm..

Still another possibility is least frequently used (LFU) Replace That block in the set that has experienced the fewest references LFU could be implemented by associating a counter with each line

A technique not based on usage. not LRU LFU FIFO or some variant is to pick a line at random ~~replacement~~ from among the

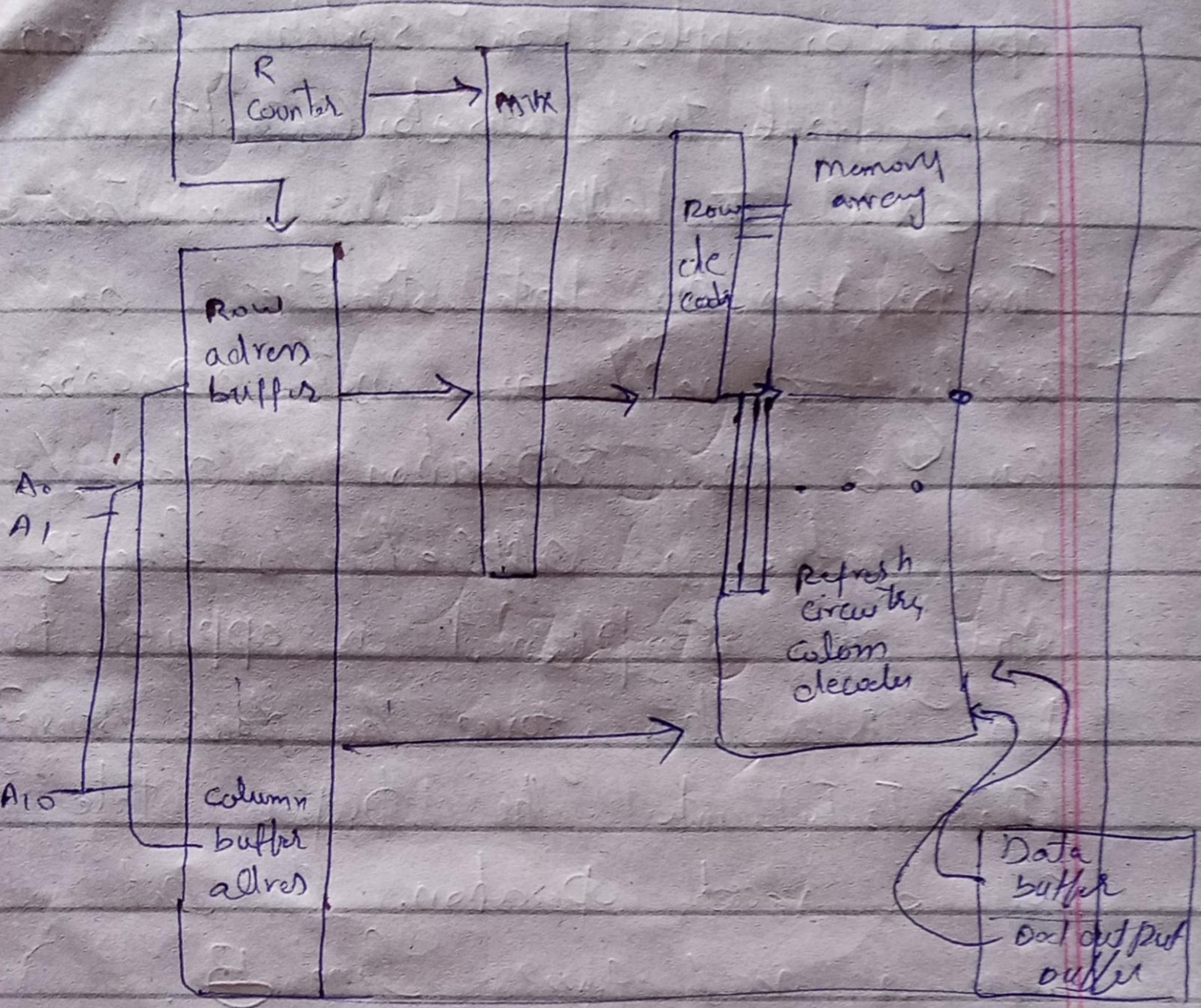
(4)

the Candidate lines.
simulation studies have shown that random replacement provides only slightly inferior performance to an algorithm based on usage [SMIT82].

(Q:No:1 par c).

The SRAM address line is used to open or close a switch. The address line control two transistor (T_5 and T_6). When a signal is applied this line the two transistor are switched on allowing a read or write operation for a write operation, the desired bit value is applied to line B while its complement is applied to line B. This forces the four transistors (T_1, T_2, T_3, T_4) into the proper state for a read operation. The bit value is read from line B.

(1(Q. No: 1) d B).
1d part)



Because only 4 bits are read/written to this DRAM. there must be multiple DRAMs connected to the memory controller to read/write a word of data to the bus. All the DRAMs require a refresh operation. A simple technique for refreshing is in effect to disable the DRAM.

(Q:NO: 1. Part e)

(1) Bits are packed more closely on a DVD. The spacing between loops of a spiral on a CD is 1.6 µm and the minimum distance b/w pits along the spiral is 0.834 µm.
The DVD uses a laser with shorter wavelength and achieves a loop spacing of 0.7 µm and a minimum distance b/w pits of 0.4 µm. The result of these two improvements is about a seven-fold increase in capacity to about 4.7 GB.

(2) The DVD employs a second layer of pits and lands on the top of the reflective layer and by adjusting focus, the lasers in DVD drives can read each layer separately.
This technique almost doubles the capacity of the disk to about 8.5 GB. The

(8)

The lower reflectively of the second layer limits its storage capacity so, That a full doubling is not achieved.

3- The DVD-Rom can be two sided whereas data are recorded on only one side of a CD.

This brings total capacity up to 17 GB.

Q:NO: 2
(Part A)

a) EEPROM and flash memory.

Flash memory is one kind of Non-volatile random access memory. It is slower than RAM but faster than hard drives. The main difference between EEPROM and Flash memory is that most EEPROM devices can erase any byte of memory at any time. Flash memory can only erase an entire "chunk" or "Sector" of memory at a time. flash memory is used primarily for storage, while RAM performs calculations on the data retrieved from storage, By their nature, flash memory and RAM are faster than storage alternatives, Such as hard disk and tape. In terms of flash memory.

(Q.NO: 2 Part B)

Hard failure and Soft error in Semiconductor memories?

In this context hard failure are errors that occur through proven defects and / or circuit bugs. hard failure or repeatable with the correct sequence of actions with in the micro controller Soft errors occur through no failure of the Circuit or defect but due to an external Source that causes the data change.

⟷

(Q, NO: 2 Part (C))

Read and write mechanism of magnetic disk.

Disk read / write heads are the small Parts of a disk drive which move above the disk plather and transform the plather's magnetic field into electrical current (read the disk) or vice versa. transform electrical current into magnetic field (write the)

(Q:No: 2. Part d)

Parallel access RAID :-

In a parallel access array all member disk participate in the execution of every I/O request. Typically, the spindles of the individuals drivers are synchronized, so that each disk hand is an in the same position on each disk at any given time.

As in the other RAID schemes data striping is used. In the case of RAID 2 and and 3, the strips are very small often as small as a single byte or word.

Independent Access RAID:- In an idependent access array, each member disk operates independently, so that separate I/O requests can be satisfied in parallel. Because of this independent access arrays are more suitable for for application that require

a high data transfer rates.
As in the other RAID schemes data stripping is used. In the case of RAID 4 through 6 the strips are relatively large.

Q:NO: 2 Part (E)

HD DVD and blue ray DVD?

Explanation. Blue ray and HD DVD both uses a blue laser which has a sholer wavelength than read ones. In contrast, HD DVDs can hold 25 GB on one layer. Even more can be packed into Blue ray / HD DVD discs if they use more than one layer or one side of the disk.

Q:NO: 3.

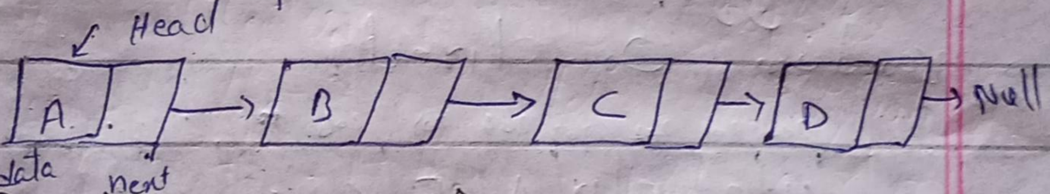
Note each of following.

a) Memory access methods:;

1- Sequential access:;

In this method, the memory is accessed in a specific linear sequential manner like accessing in a single linked list.

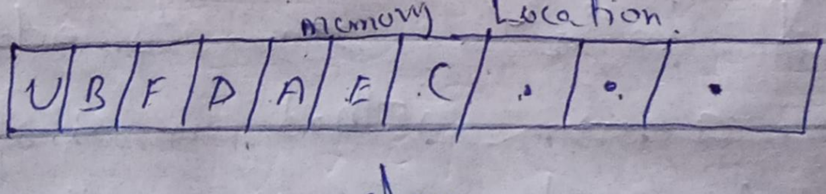
Application of this sequential memory access are magnetic tapes, magnetic disk and optical memories.



2- Random access.

In this method, any location of the memory can be accessed randomly like accessing in Array. Physical location are independent in this access method.

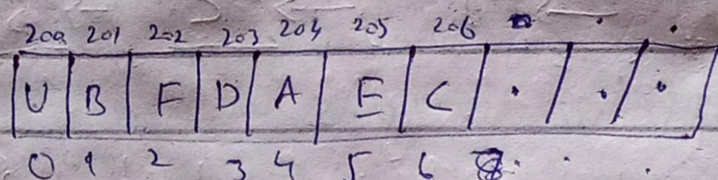
Application of this method access are RAM and ROM



Q: NO: 3.

3- Direct access:;

In this method the particular location of the memory can be accessed directly like accessing in Array. This method is a combination of above two access methods. The access time depends on the both the memory organization and characteristics of storage technology. The access is semi-random or direct.



Application of thus direct memory access is magnetic hard disk, read /write header.

4- Associative access;

In this memory, a word is accessed rather than its address. This access method is a special time of random access method. Application of thus direct memory access is cache memory.

(Q: No: 3 Part b)

Principal of locality:;

In Computer Science locality of reference also known as principal of Locality.

① It is the tendency of Processor to access the Same set of memory location repetitively over a short period of time.

② There are two basic types of reference locality. Temporal and spatial locality.

③ refer to use of data elements with in a relatively small element with in relatively close storage location. Sequential locality a special case spatial locality occurs when data elements are arranged and accessed linearly such as traversing the elements in One dimensional array.

possible approaches of cache coherance.

! (QNO: 3: part C)

In computer architecture, cache coherance is the uniformly of shared resources data that ends up stored in multiple local caches when clients in a system maitain caches of a common memory resources, problems may rise with incoherant data which is particularly the case with CPUs in a multi-processing system.
In the ilustration on the right consider both the clients have a cached copy of a particular block from a previous read. Suppose the client on the button on the top could be left with in an invalid cache of memory without any notification of the change. cache coherance is intended to manage such conflicts by maintaining a coherent view of the data values in multiple caches.

(Q:NO: 3. Part d)

There are two practical issues peculiar to SSDs that are not faced by HDDs
SSD performance has a tendency to slow down as the device is used.

- The entire block must be read from the flash memory and placed in a RAM buffer.
- Before the block can be written back to flash memory.
- Flash memory become unussable after a certain number of writes.
- Techniques for prolonging life.
Front-ending the flash with a cache to delay and group write operation.
- using wear leveling algorithms That evenly distributes write accross block of cells.
Bad-block management techniques.
most flash devices estimate their own remaining lifetimes so system can participate failure and take preeptive action.

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(Q:NO: 3 Part E)

Discuss the CD read and write.

Read.

Information is retrieved from CD or CD-ROM by a low powered laser housed in an optical disk player or drive unit. The laser shines through the clear polycarbonate while a motor spins the disk past it. The intensity of the light reflected of the laser changes as it encounter a pit. Specifically if the laser beam falls on a pit which has a somewhat rough surface the light scatters and a low intensity is reflected back to source. The area between pits are called lands. A land is a smooth surface which reflects back at higher intensity. The change between pits and lands is detected by a photo sensor and converted into a digital signal. The sensor tests the surface at ragular intervels. The begining or

end of ~~or~~ a pit represents a 1
when no change in elevation occurs
between intervals a 0 is recorded

Write.

Recall that on a magnetic disk, information is recorded in concentric tracks with the simplest constant angular velocity (CAV). The number of bits per track constant. An increase in density is achieved with multiple zoned recording in which the surface is divided into a number of zones with zones further from the center containing more bits than zones closer to the center.

Although this technique increases capacity. It is still not optimal

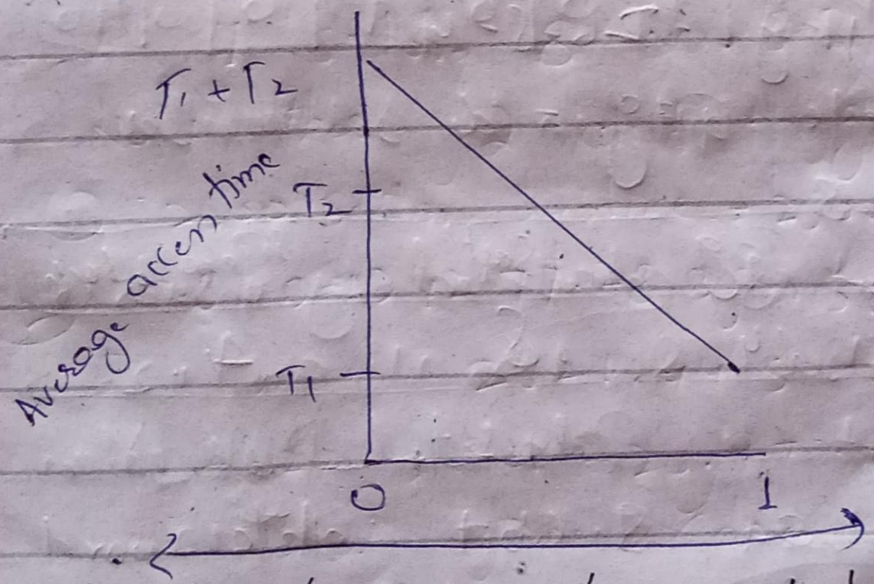
((Q:NO:4) Part a)

Suppose 95% of the memory access are found in level 1. then The average time to access a word can be expressed as

$(0.95)(0.01 \mu s) + (0.05)(0.01)\mu s + (0.1 \mu s) =$

$= 0.0095 + 0.0055 = 0.015 \mu s$

The average access time is much closer to $0.01 \mu s$ than $0.1 \mu s$ as desired



((Q:NO: 4 part b)

Total blocks in the cache =

$= 8k \text{ bytes} / 16 \text{ bytes} = 2^3 \times 2^{10} / 2^4 = 2^9 = 512$

number of set = number of blocks in cache / 2

(20)

Tag set and word

Tag (1) | set (8) | word (2) 177H/0EEH/3H

number of set = 512/2

number of set in Cache = 256

number of set in Cache = 2^8

No of set = 8

size block = 16 = 2^4

size of memory = $2^6 \times 2^{20} = 2^{26}$

Type size of memory - set size of block

Tag = size of memory - set - size of block

Tag = 26-8-4

Tag = 14

Tag	Set	Size of block
14	8	4.

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(Q: NO: 4 d)

7200 revolution in 60 sec

1 revolution in 60/7200 OR

1 revolution = Conveying One entire track = 500 Sector

500 sector = 6 ms

1 sector = 8 micro Second.

Now there 2 diff things

(1) 2500 Sector. So time = 2500 × 8 ms = 20 ms

(2) 1.28 mB = 1342177.28 Bytes or

2621.44 Sectors.

2622 sector = 20.97 ms.

Total time case

Case (1) 4 + 2 + 20 = 26 ms

Case (2) 4 + 2 + 20.976 = 26.97 ms

(Q. NO. 4 part C)

suppose an 8-bit data word stored in memory is 10101010. Using the hamming code determine what check bits would be stored in memory with the data word.

$M = 8$

$2^k - 1 >= k + m$

$2^4 - 1 >= 4 + 8$

$15 >= 12$

1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	1	1	0	0	1	0	0	1	0

The check bit in a bit number 1, 2, 4, 4, 8.

- check bit 8 calculated by values in bit number 9, 10, 11, and 12
- Check bit 4 calculated by value in bit number 5, 6, 7, and 12.
- Check bit 2 calculated by values in bit number 3, 6, 7, 10, and 11
- check bit 1 calculated by values in bit number 3, 5, 7, 9, 10, and 11

Thus the check bit are : 1011

END