DATA LOGIC & DESIGN (Final Term Paper)

ID: 12290

Student Name : AAMIR SALEEM
Student ID : 12290
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Instructor : Sir Muhammad Ameen
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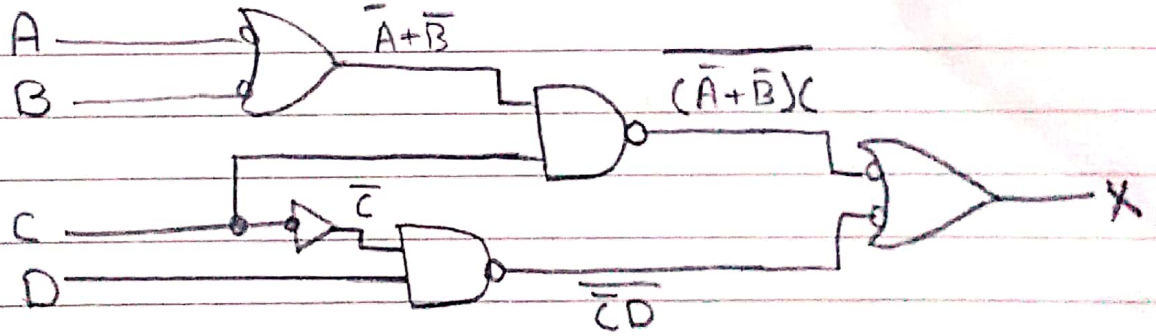
Q1 Draw the logic circuit using the input (A, B, C, D) & output (x) waveforms in Fig 01.

Solution:



So,

$$X = \overline{\overline{(\overline{A}+\overline{B})C} + \overline{\overline{C}D}} = (\overline{A}+\overline{B}) + \overline{C}D = \overline{A}C + \overline{B}C + \overline{C}D$$

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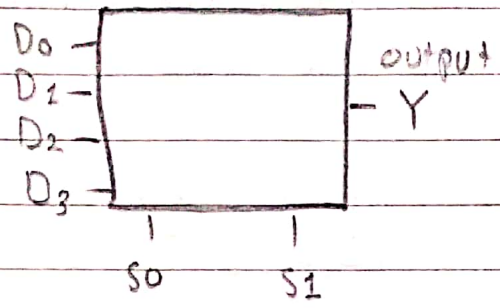
Q2 For the 4-input multiplexer data inputs are

$D_0 = 0$, $D_1 = 1$, $D_2 = 0$, $D_3 = 1$.

Solution:

We use 4x1 multiplexer

Block diagram:



Truth table:

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Finding Output Y

S_0	S_1	Output
1	0	$D_2 = 0$
0	1	$D_1 = 1$
1	1	$D_3 = 1$
0	0	$D_0 = 0$

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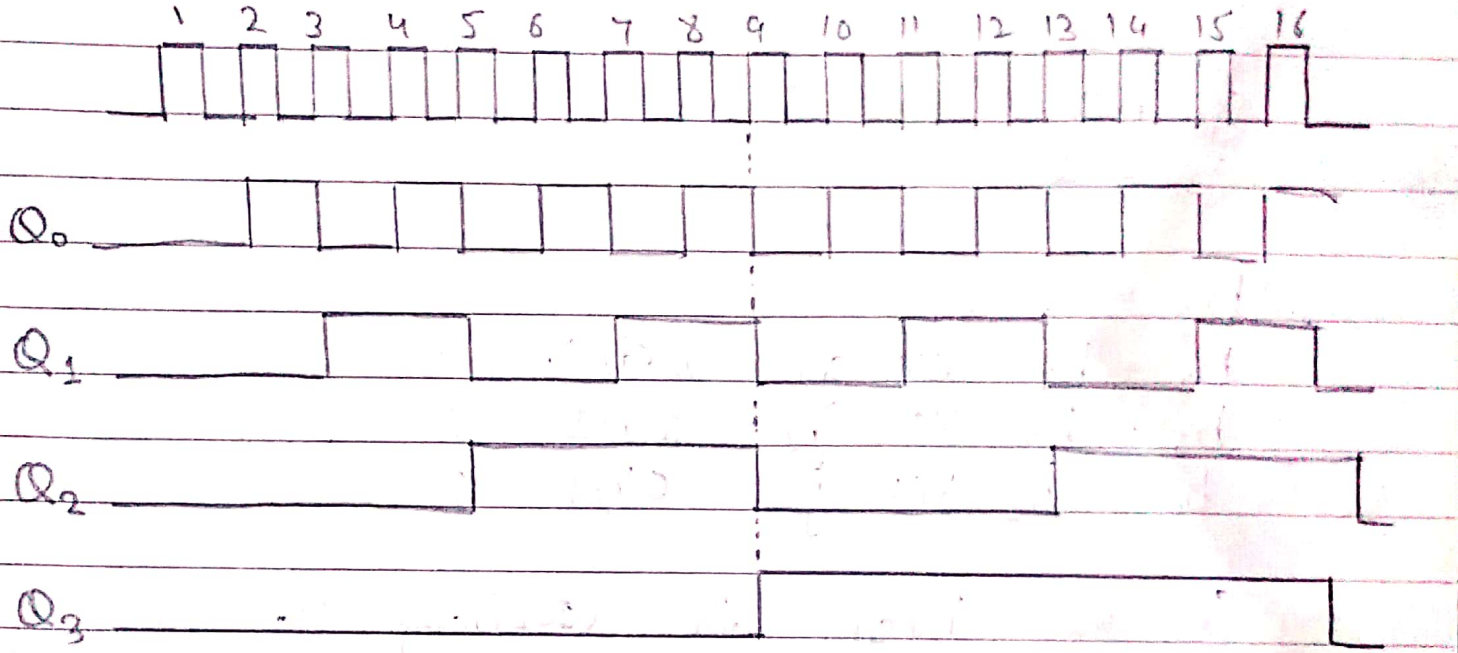
Q4 = Draw logic diagram & timing diagram for 4-stage synchronous binary counter.

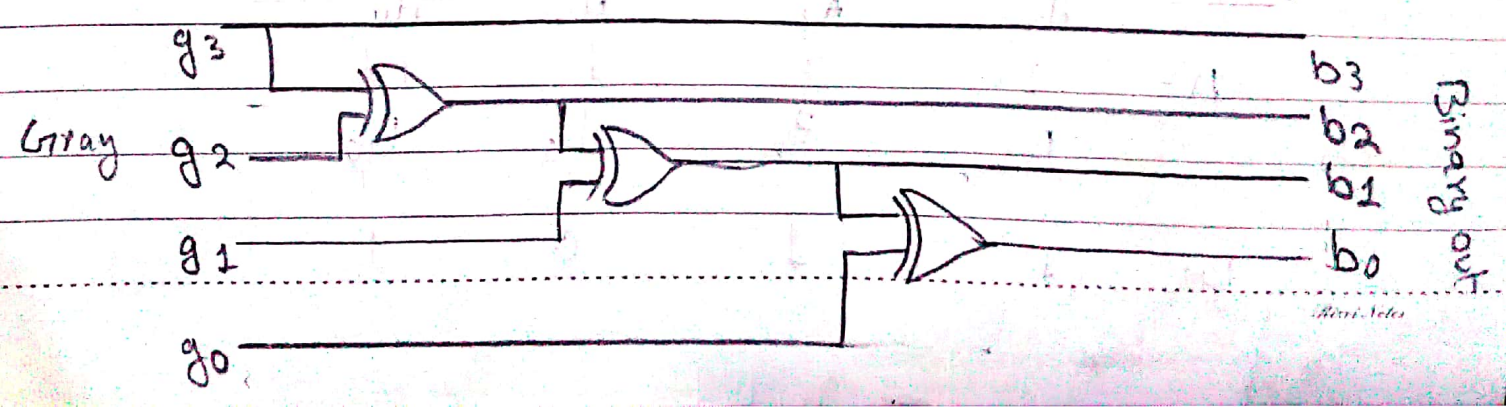


Count 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Q5 Show logic required to convert a 4-bit gray code to binary & use that logic to convert following : 1011

Solution:-

Logic diagram for 4-bit gray to binary =



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Gray code =

1011.

$g_0 = 1$
$g_1 = 1$
$g_2 = 0$
$g_3 = 1$

$b_3 = g_3 = 1$
$b_2 = b_3 \text{ XOR } g_2 = 1 \oplus 0 = 1$
$b_1 = b_2 \text{ XOR } g_1 = 1 \oplus 1 = 0$
$b_0 = b_1 \text{ XOR } g_0 = 0 \oplus 1 = 1$

So the bingry for $(1011)_{Gray}$ is =

1101 Answer.

Q4. Determine the A = B, A > B, & A < B output for the input numbers shown .....

Solution:-

A > B = 1 (true)
A = B = 0 (Not true)
A < B = 0 (Not True)

	A_3	A_2	A_1	A_0
A =	1	0	1	0
	B_3	B_2	B_1	B_0
B =	1	1	0	1

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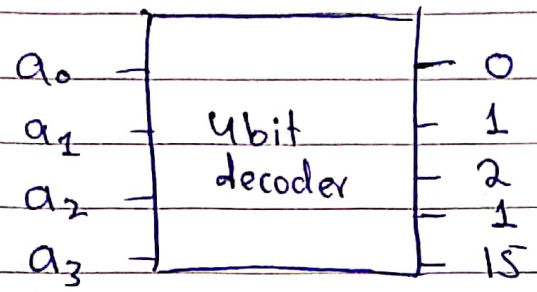
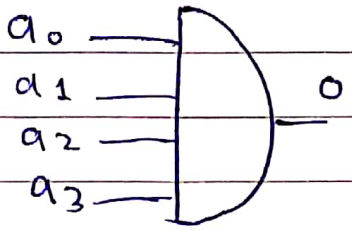
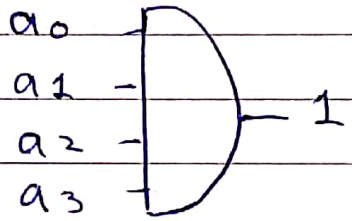
Q6 4-bit Decoder?

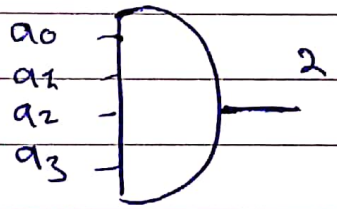
Answer:-



Logic diagram:-







. . . . .

Expression:-

$0 = \overline{a_3}\,\overline{a_2}\,\overline{a_1}\,\overline{a_0}$

$1 = \overline{a_3}\,\overline{a_2}\,\overline{a_1}\,a_0$

$2 = \overline{a_3}\,\overline{a_2}\,a_1\,a_0$

$3 = \overline{a_3}\,\overline{a_2}\,a_1\,a_0$

$4 = a_3\,a_2\,\overline{a_1}\,\overline{a_0}$

$5 = \overline{a_3}\,a_2\,\overline{a_1}\,a_0$

$6 = \overline{a_3}\,a_2\,\overline{a_1}\,a_0$

$7 = \overline{a_3}\,a_2\,a_1\,a_0$

$8 = a_3\,\overline{a_2}\,\overline{a_1}\,\overline{a_0}$

$9 = a_3\,\overline{a_2}\,a_1\,\overline{a_0}$

$10 = a_3\,\overline{a_2}\,a_1\,\overline{a_0}$

$11 = a_3\,\overline{a_2}\,a_1\,a_0$

$12 = a_3\,a_2\,\overline{a_1}\,\overline{a_0}$

$13 = a_3\,a_2\,\overline{a_1}\,a_0$

$14 = a_3\,a_2\,a_1\,\overline{a_0}$

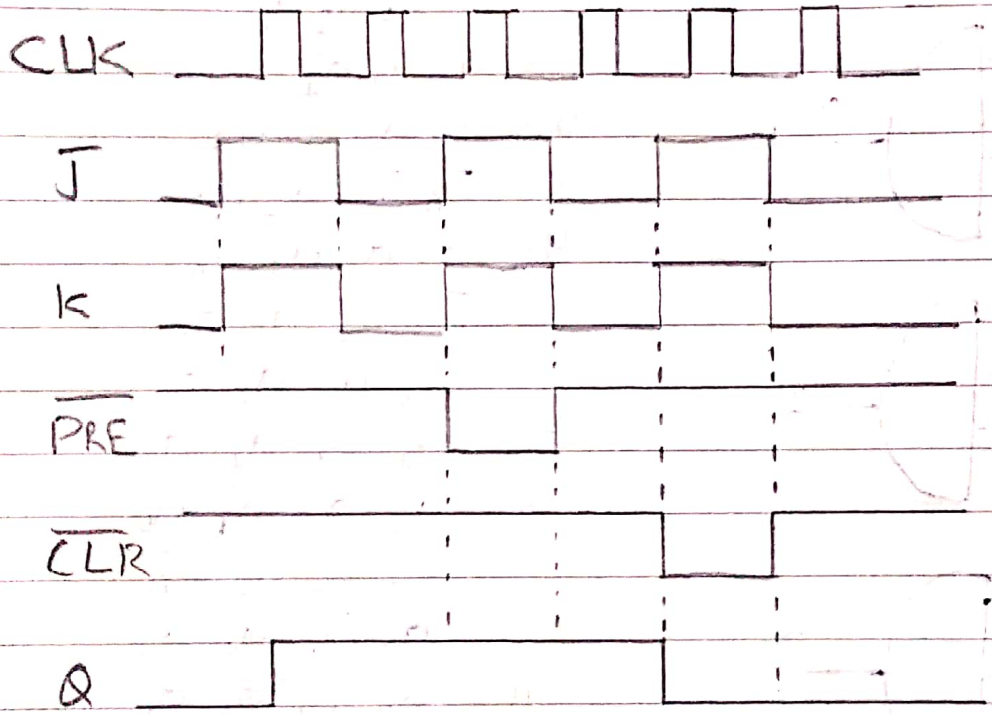
$15 = a_3\,a_2\,a_1\,a_0$

Subject:

DLD (Final)

Q7 Draw & explain logic diagram for frequency divider (use 3 J-K flip flops).

Q8 Determine the Q waveform relative to the clock if the signals shown in fig are applied.....



Truth table

Clk	J	K	PRE	CLR	Q
1	1	1	1	1	1
2	0	0	1	1	1
3	1	1	0	1	1
4	0	0	1	1	1
5	1	1	1	0	0
6	0	0	1	1	0

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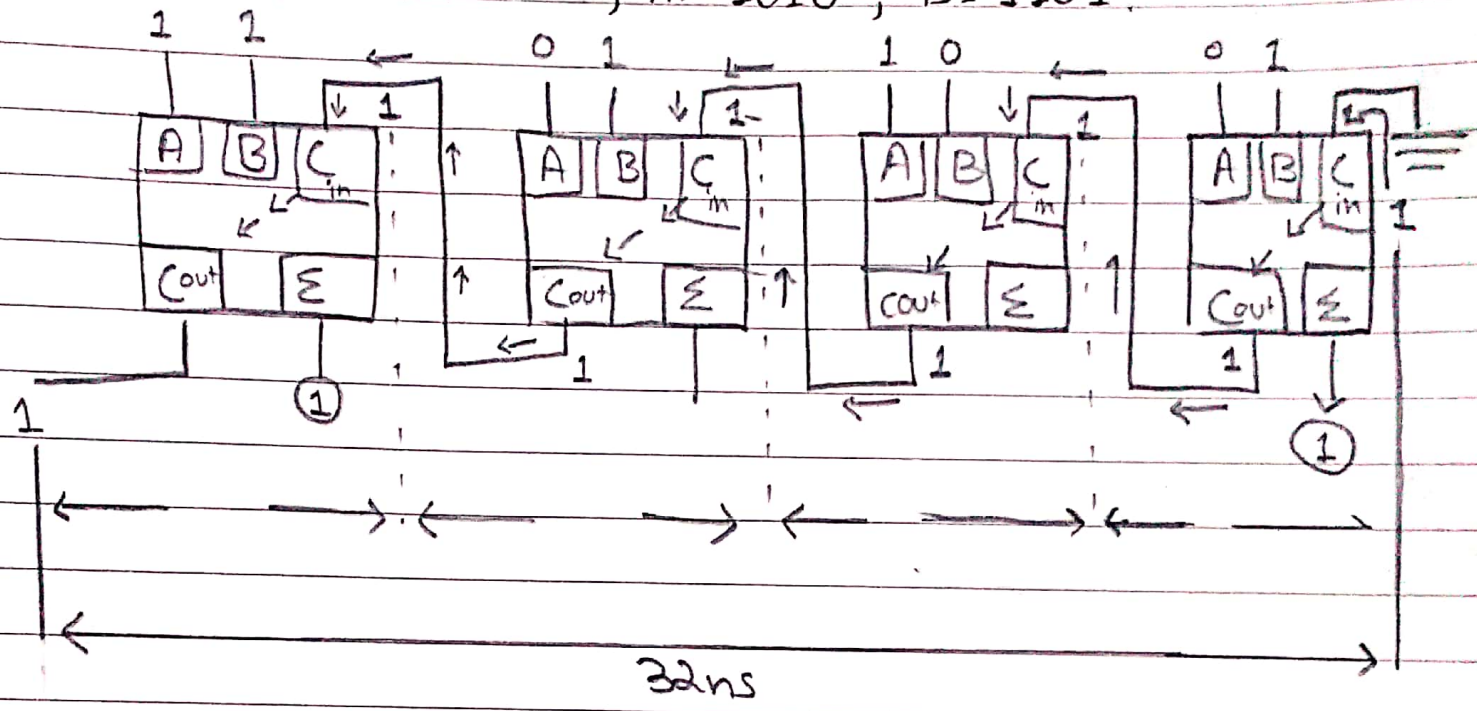
DLD Final.

Q3 For the circuit assum the inputs are $\overline{Add}/Subt = 1$, A= 1010 , B= 1101.



The answer is 1101.

Finish.