

Digital Logic Design

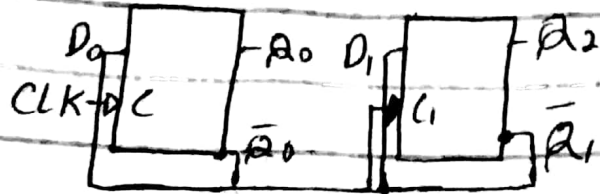
Six. Muhammad Amin

Muhammad YASIR

15459

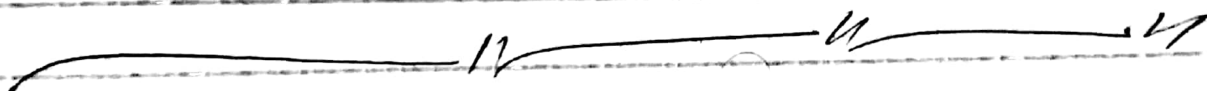
Assignment # 08

Question - No - 01 A



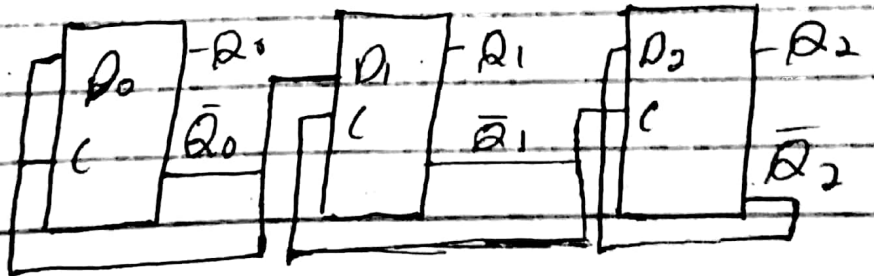
Soln

CLK	1	2	3	4	Clock Phase	Q1	Q0
$\bar{Q}_0$	0	1	0	1	initially	0	0
Q0	1	0	1	0	1	0	1
Q1	0	1	0	1	2	1	0
					3	1	1
					4	0	0



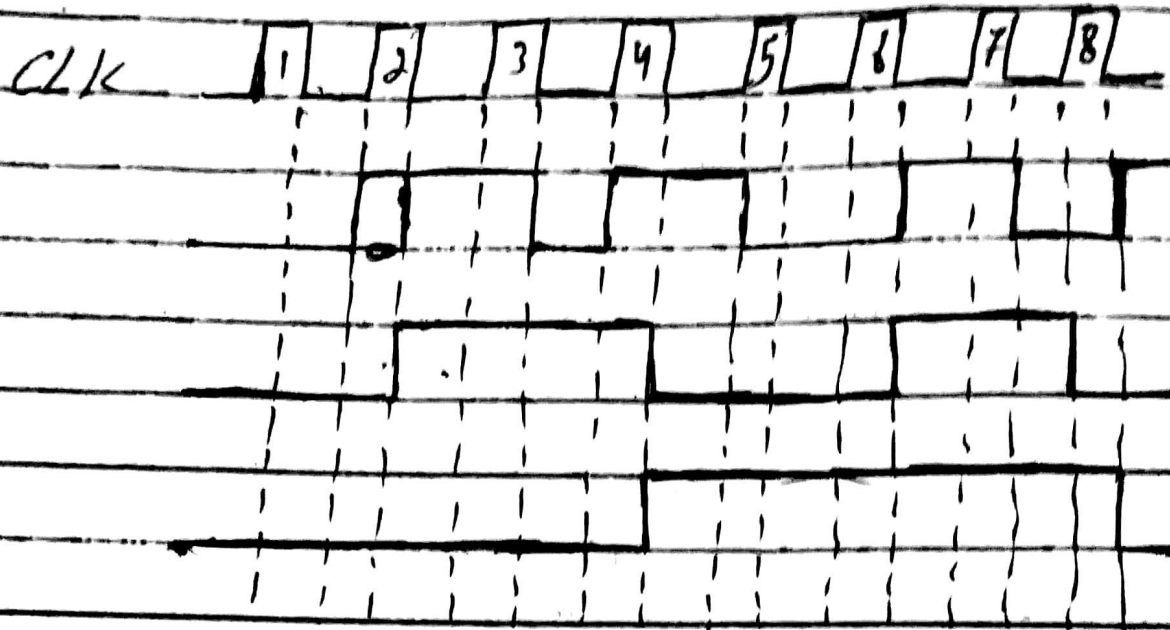
Question - No - 02 A

CLK



1	2	3	4	5	6	7	8	C Pulse	Q2	Q1	Q0
								initially	0	0	0
								1	0	0	1
								2	0	1	0
								3	0	1	1
								4	1	0	0
								5	1	0	1
								6	1	1	0
								7	1	1	1
								8	0	0	0

Q3)



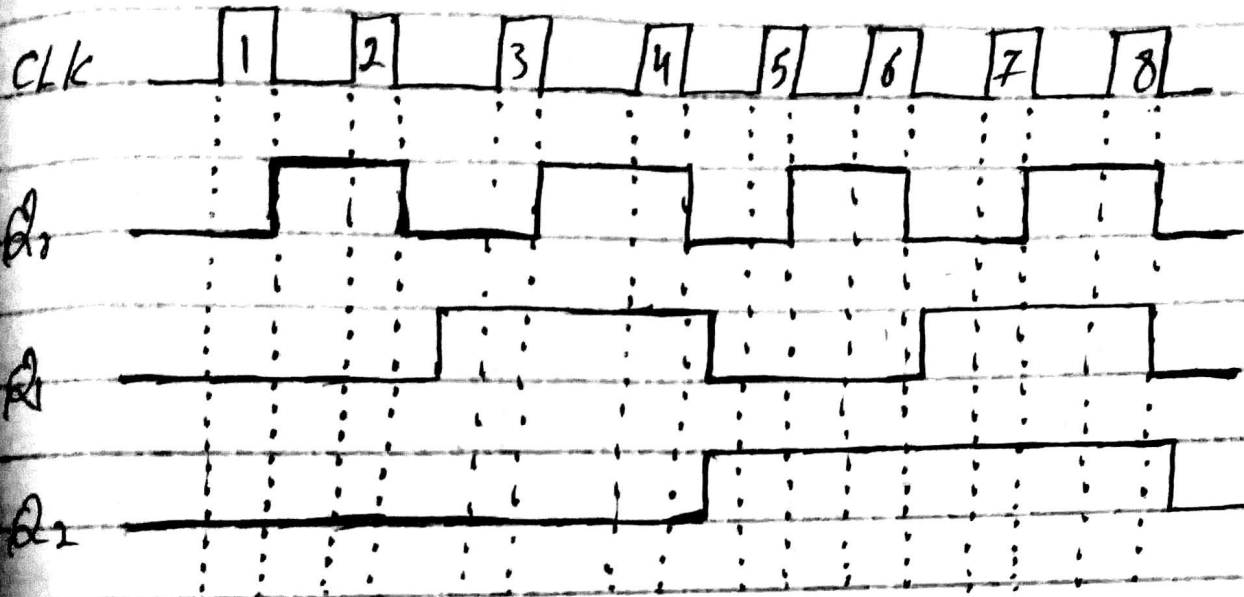
The worst case delay occurs on

CLK - Q<sub>0</sub>

The highest delay 8ns, because in the case of synchronous binary, the propagation delay is independent of the number of flip-flops used

Q4)

## Asynchronous

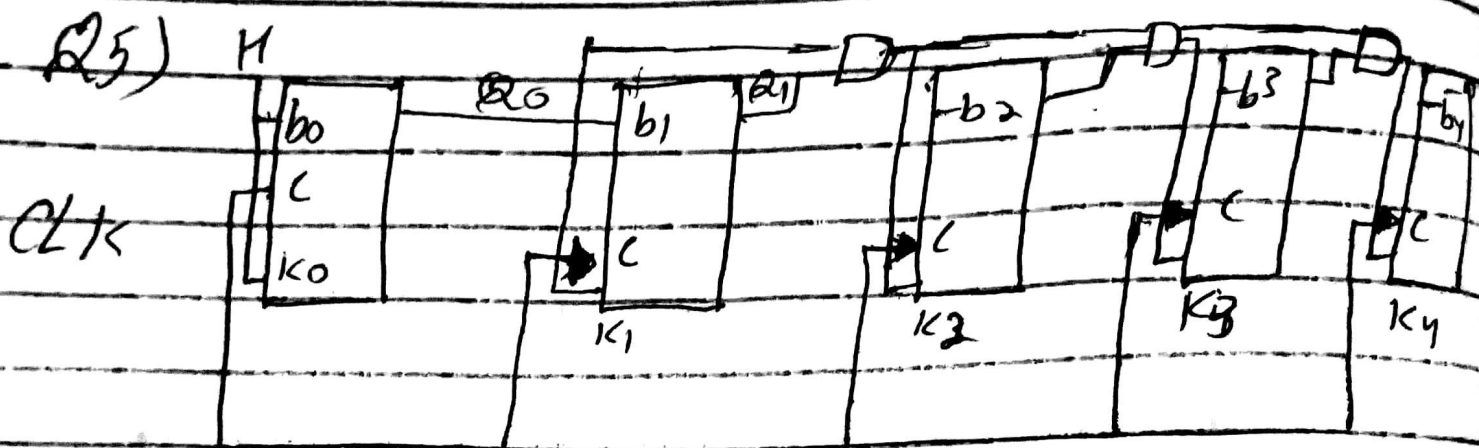


The worst case delay time occurs at Q<sub>2</sub>.

The delay interval equals to three times the delay time at Q<sub>2</sub>.

$$3(8\text{ns}) = 24\text{ns}$$

24



CLK

1	2	3	4	5	6	7	8
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$Q_0$

$Q_1$

$Q_2$

$Q_3$

$Q_4$

C. Pulse	$R_0$	$R_1$	$R_2$	$R_3$	$R_4$
initially	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0
21	1	0	1	0	1
22	1	0	1	1	0
23	1	0	1	1	1
24	1	1	0	0	0
25	1	1	0	0	1
26	1	1	0	1	0
27	1	1	0	1	1
28	1	1	1	0	0
29	1	1	1	0	1
30	1	1			