Final Term Summer

Course Name: Digital Logic Design

Submitted By:

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BS (SE-8) Section: A

Submitted To:

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Department of Computer Science,
IQRA National University, Peshawar Pakistan

Digital Logic & Design/Digital Systems

Programs: BS (CS) /BS (SE) /BS (TELC)

Course Codes: CSC-201/ SEC-201/TSC-201

EDP Codes: 102007016
Instructor: Muhammad Amin
Examination: Final Term
Semester: Summer 2020
Date: Sep. 26, 2020
Timing: 3:00 pm – 7:00 pm

Question No.	Q.1	Q.2	Q.3	Q.4	Q.5	Q.6	Q.7	Q.8	Q.9	
Total Marks	5	5	5	5	6	6	6	6	6	50

Note: Attempt all questions.

Q.1 Draw the logic circuit using the input (A, B, C, D) and output (X) waveforms in Figure 01.

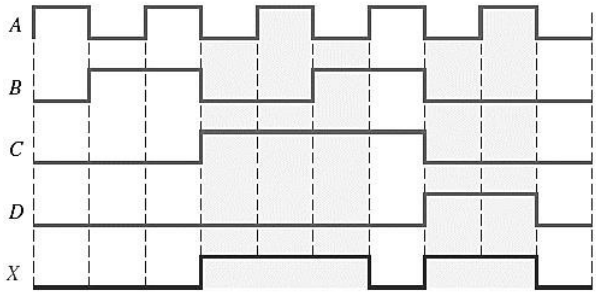


FIGURE 01

Q.2 For the 4-input multiplexer, data inputs are given as:

$D_0 = 0, D_1 = 1, D_2 = 0, D_3 = 1$

Find the output Y if the select inputs are given as:

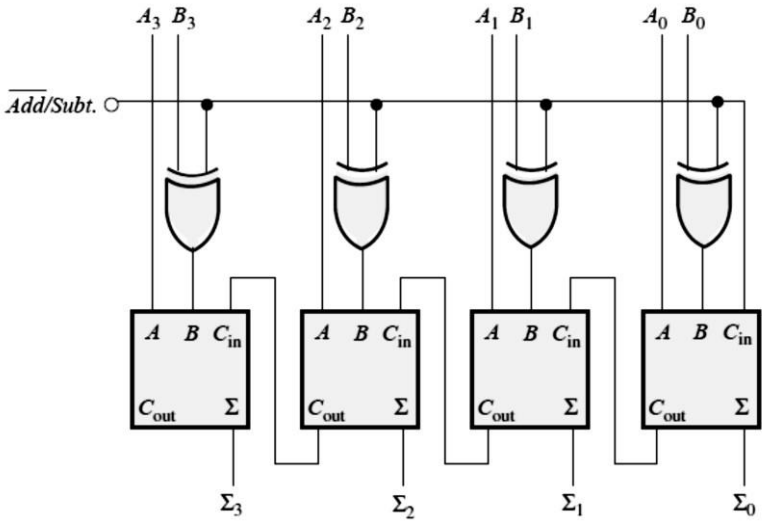
a) $S_0 = 1, S_1 = 0$

b) $S_0 = 0, S_1 = 1$

c) $S_0 = 1, S_1 = 1$

d)$S_0 = 0, S_1 = 0$

For the circuit in Figure 02 , assume the inputs are $\overline{Add}/Subt. = 1$, $A = 1010$, and $B = 1101$.



Q.3

What is the output?

FIGURE 02

Q.4 Determine the A = B, A > B, and A < B outputs for the input numbers shown on the comparator in Figure 03.

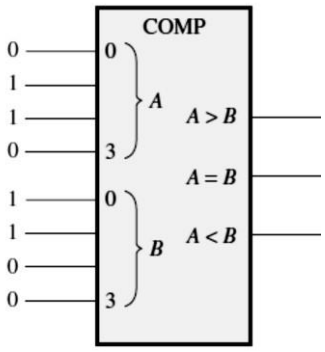


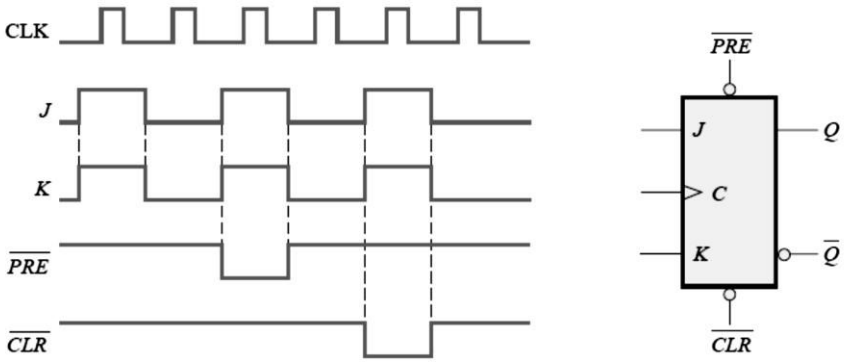
FIGURE 03

Q.5 Show the logic required to convert a 4-bit Gray code to binary and use that logic to convert the following Gray code words to binary: 1011

Q.6 Draw and explain the logic diagram for 4-bit active low decoder.

Q.7 Draw and explain the logic diagram for frequency divider (Use 3 J-K flip-flops and assume 16 kHz frequency of the initial wave-form.)

Q.8 Determine the Q waveform relative to the clock if the signals shown in Figure 04 are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW.



Q ----------?

FIGURE 04

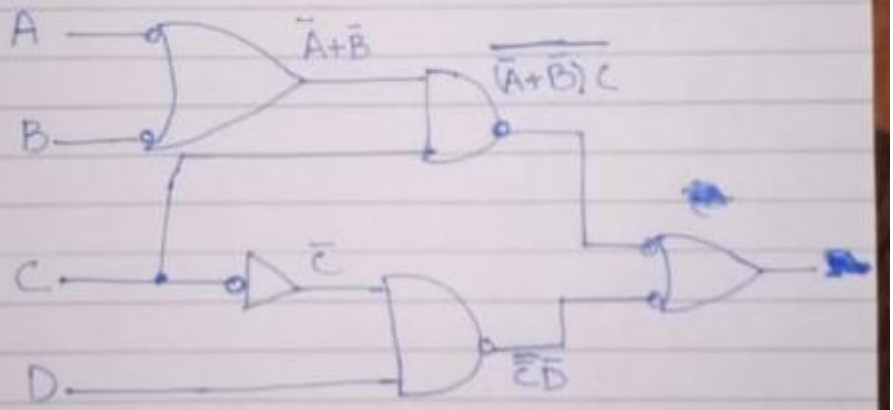
Q.9 Draw the logic diagram and timing diagram for the 4-stage synchronous binary counter. Verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.

*********End of Exam*********

Answer No 1:

Q1)

Ans) The output expression for the development circuit is developed in . The SOP form indicates that the output is HIGH when A is low C is HIGH or when B is low and C is HIGH or when C is low and D is HIGH.



$$X = \overline{(\bar{A}+\bar{B})C} + \overline{\bar{C}\bar{D}} = (\bar{A}+\bar{B})C + \bar{C}\bar{D} = \bar{A}C + \bar{B}C + \bar{C}\bar{D}$$

Answer No 2:

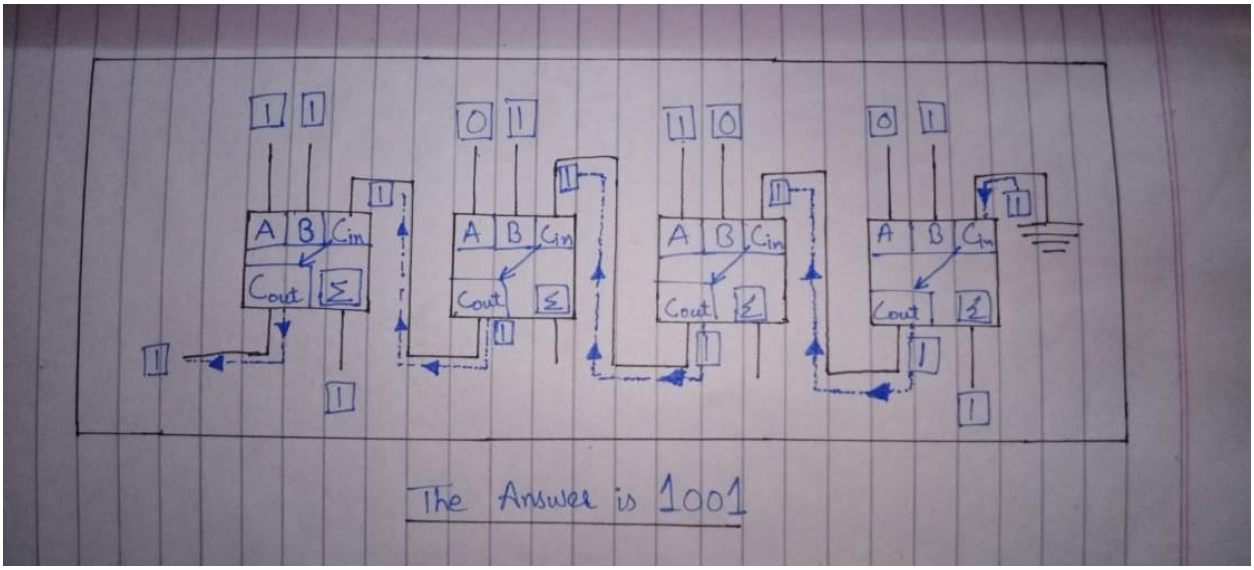
Q2

ANSWER:-

The truth table of a 4 to 1 multiplexer is shown below in which four input combinations 00, 10, 01 and 11 on the select lines respectively switches the inputs D_0, D_2, D_1 and D_3 to the output. That means when $S_1 = 0$ and $S_0 = 0$, the output at Y is D_3, similarly Y is D_0 if the select inputs $S_1 = 0$ and $S_0 = 1$ and so on.

Select		Data Input	output
S_1		S_0	Y
0		0	D_3
0		1	D_0
1		0	D_1
1		1	D_2

Answer No 3:

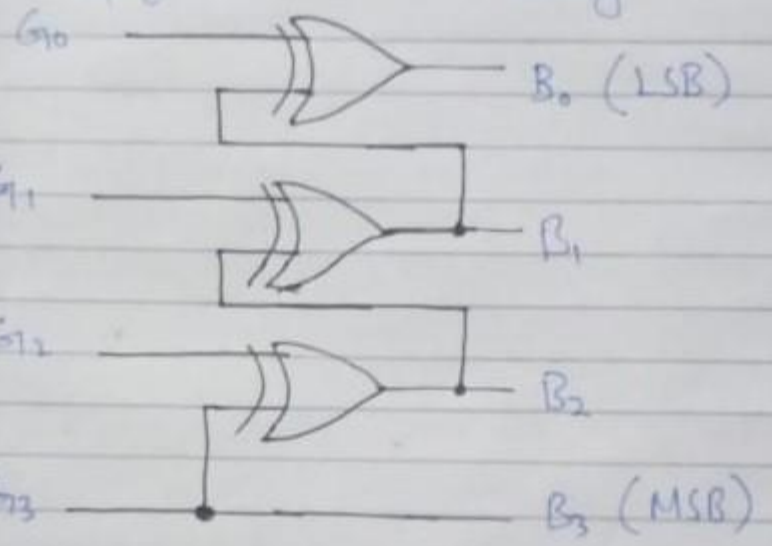


Answer No 4:

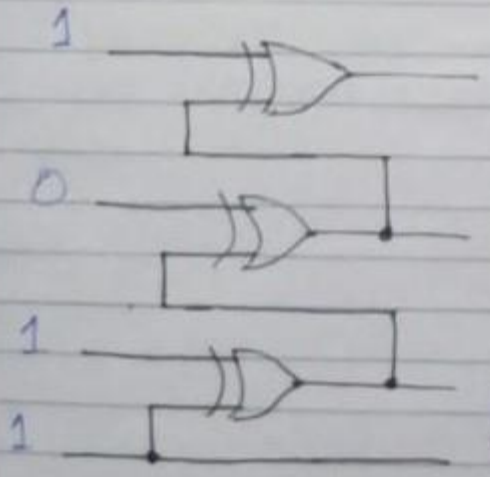
The number on A inputs is 0110 and the number on B is 0011. The A>B output is I and the other inputs are LOW.

Question 5

The Logic for Converting 4-bit gray → binary

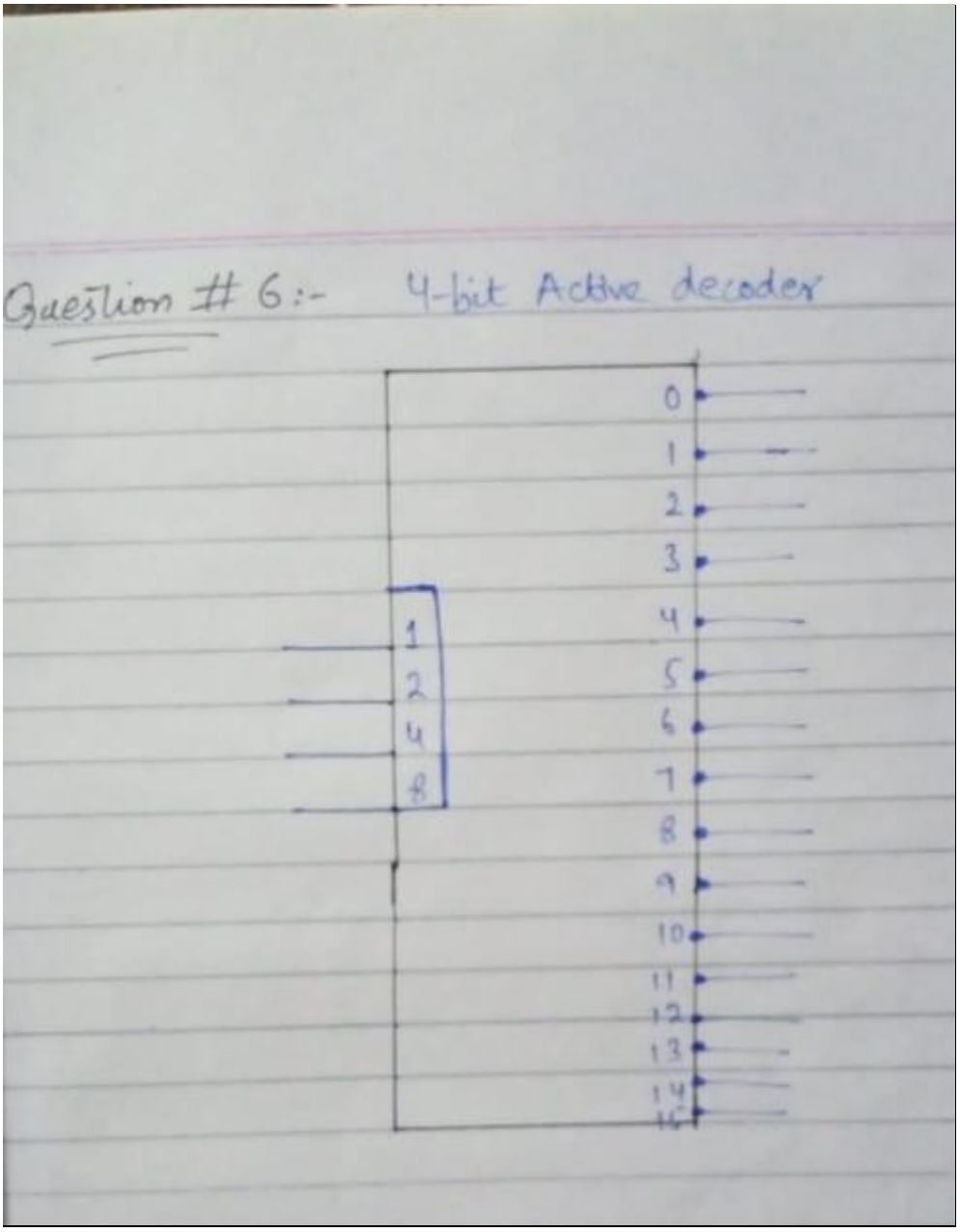


→ Now converting 1011 gray code into binary. Which is $(1101)_2$ binary.



→ The Answer is $(1101)_2$.

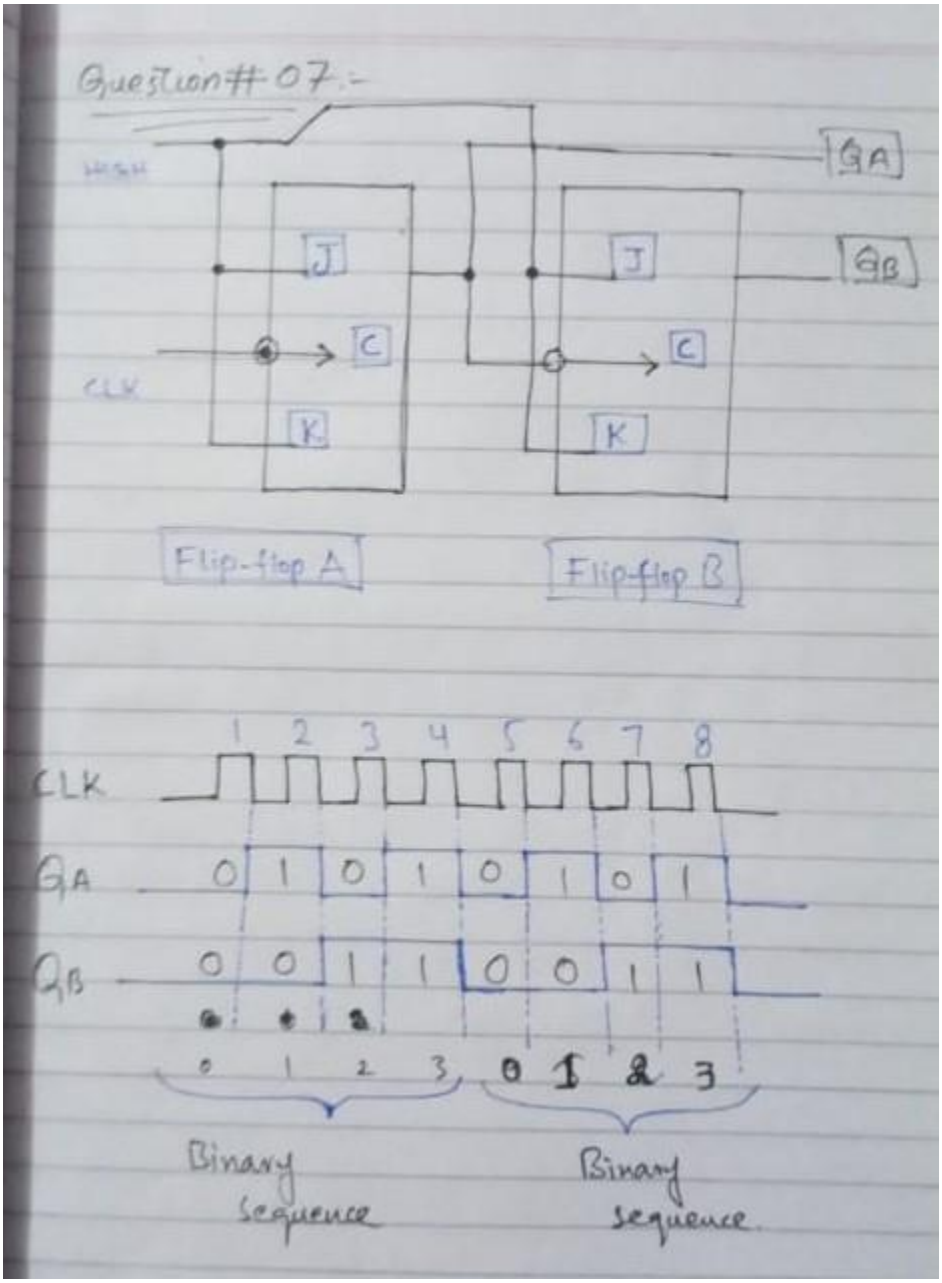
Answer No 6:


Question # 6:- 4-bit Active decoder
1
2
4
8
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

The 4-bit decoder in order to decode all possible combination of four bits, sixteen decoding gates are= 16. This type of decoder is commonly called either a 4 line to 16-line decoder because there are four inputs and 16 outputs or a 1 to 16 decoder because for any given codes on the inputs, one of the 16 outputs is activated. A list of sixteen binary codes and their corresponding functions is given in diagram.

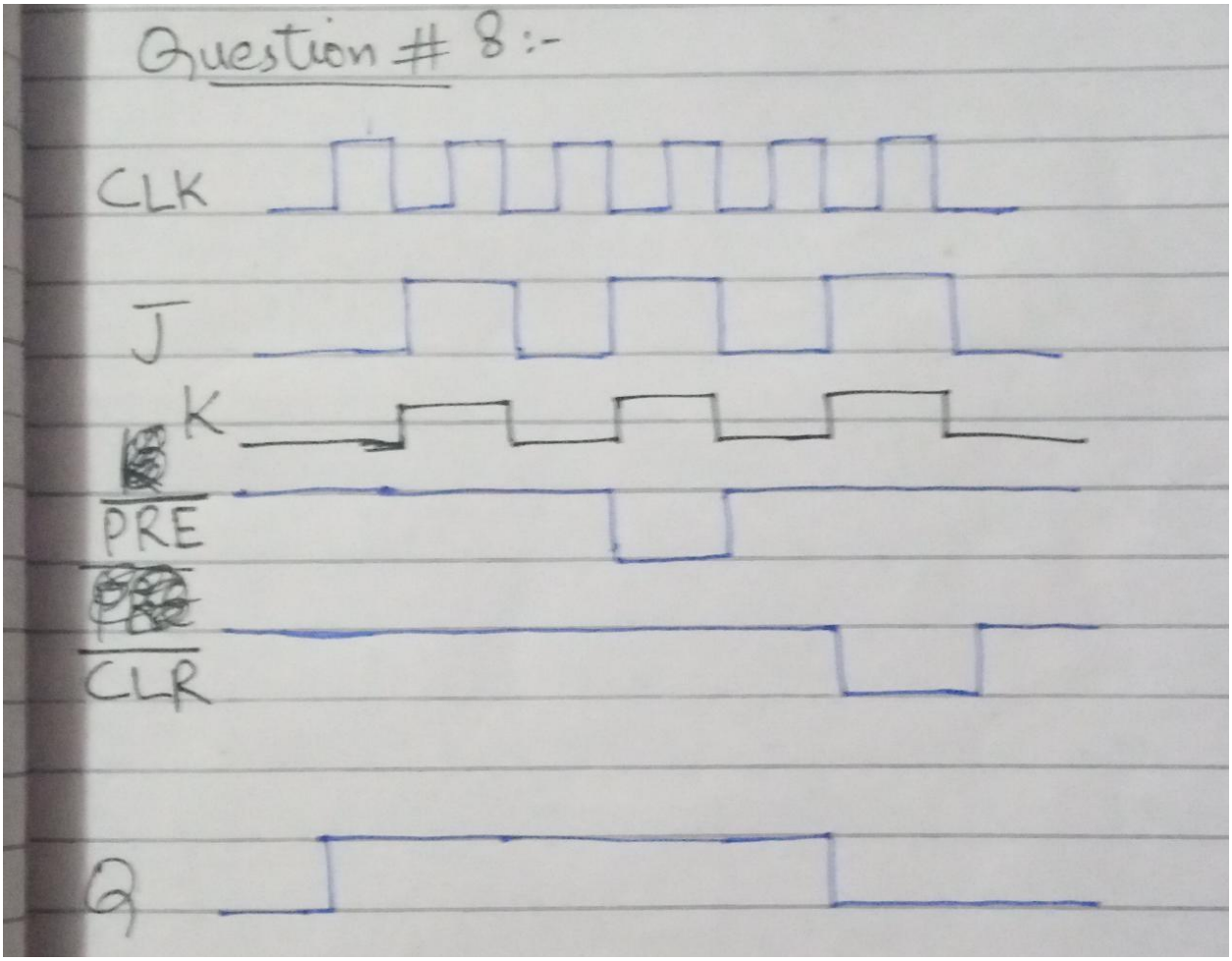
If an active LOW output is required for each decoded number, the entire decoder can be implemented with NAND gate and inverters. In order to decode each of sixteen binary codes, sixteen NAND gates are required (AND gates can be used to produce active HIGH outputs). A logic symbol from 4 line to 16-line decoder with active LOW outputs is shown in the diagram. The BIN/DEC indicates a binary input makes the corresponding decimal output active.

Answer No 7:


Question # 07 :-
HIGH
CLK
J
C
K
J
C
K
QA
QB
Flip-flop A
Flip-flop B
1 2 3 4 5 6 7 8
CLK
QA
QB
0 1 0 1 0 1 0 1
0 0 1 1 0 0 1 1
0 1 2 3 0 1 2 3
Binary sequence
Binary sequence

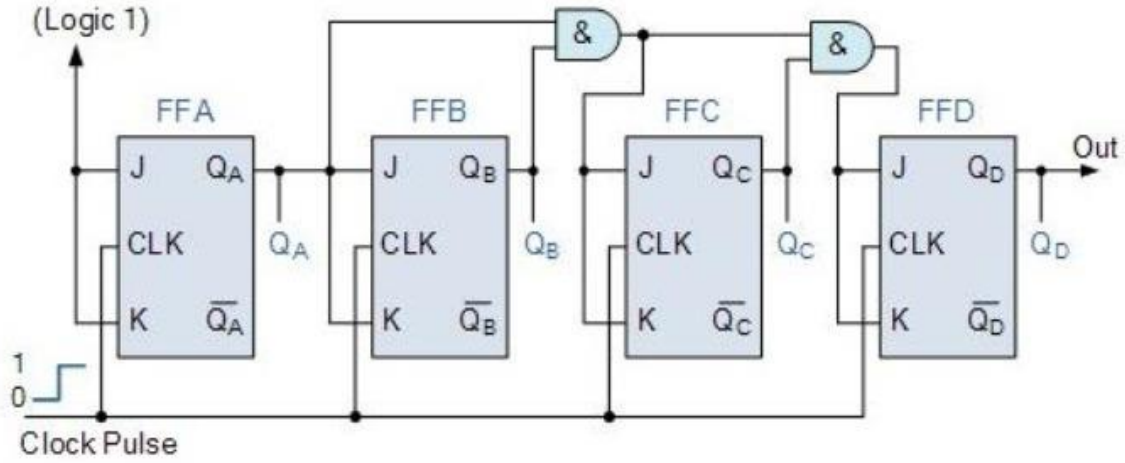
The logic diagram for frequency divider using 3 J-K flip flops and assume 16 kHz frequency of the initial wave form. The negative edge triggered J-K flip flops are used for illustration. Both flip-flops are initially RESET. Flip-flop of A toggles on the negative going transition of each clock pulse. The Q output of flip-flop A clocks flip-flop B, so each time QA makes a HIGH to LOW transition, flip-flop B toggles. The resulting QA and QB are shown in the diagram.

Answer No 8:



Answer No 9:

Logic Diagram for 4-stage Synchronous Binary Counter



Timing diagram for the 4-stage Synchronous Binary Counter