NAME	M. Bilal
ID	14726
Dept	BS(cs)
Semester	4th
Assignment No	1
Subject	Computer Architecture

ID 14726

Q1
a
Ans:

Data Processing:
Data may take a wide variety of forms and the range of processing requirement is broad.

Data Storage:
The computer perform a long term data storage on the computer for subsequent retrival & update

Data Movement:
When data are moved over longer distance to or from a remote device the process is know as data communication.

Control:
This with in the Computer a Control unit manages.

B)
Ans:-

Instruction Sequence Units:

Determines the Sequence in instruction are executed in what is referred to as a Superscalar architecture.

Instruction fetch Unit:- Logic for fetching instructions.

Instruction decode Units.

The IDU is fed from the IFU buffer and is responsible for the parsing and decoding of all x/Arch operation code.

Load Storage Units:-

It is responsible for handling all types of operand accesses of all length mode and formats.

XU (translation Unit):

This unit translate logic address from instruction into physical address in main memory.

Fixed Point Unit:

The fixed point Unit executed fixed point arithmetic operation.

Binary floating Point Unit:

The Binary floating Point Unit all binary and hexadecimal floating point operation

Decimal floating Point Unit:

The Decimal floating Point Unit handle both fixed Point and floating Point operation numbers that are stored decimal digits.

Recovery Unit:

The Recovery unit keep a copy of the complete State of the system

that include all register.

CoP :

The Cop is responsible for data compression and encryption function are each core.

L_2 Controller

This is the control that manage the traffic through the two L_2 caches.

Data L_2 :

A 1-MB L_2 Data Cache for all memory traffic other than.

C)

Ans :

The IAs operates by respectively performing its instruction cycle. Each instruction cycle consist of two subcycle.

Fetch Cycles
Execute

The control circuitry interpretes the opcode and executed the instruction by sending out the appropriate

Control Signal to Cause data to be moved an operation to be Perform by the ALU.

a)
Ans:

No these Program are never Considered to be embedded because they are not an integral Component of large System.

b)
Ans:

Yes, Regardless of what the disk drive is used for the Software with in the disk drive Controls the head disk assembly hardware and is hard real time as well.

c)
Ans:

No, Input Output drivers do not represent the embedded System is a ~~x~~ (Personal digital ~~Assistant~~ Assistant an embedded System) x

d)
Ans:
Yes. PDA is an embedded System because it is just like a Personal Computer in hand.

e)
Ans:
Yes, the firmware in the Cell phone is Controlling the radio hardware.

F)
Ans:
Yes. these Computer were generally Some of the most Powerfull Computer avaible when the system was built in a located in a large Computer room. occupy almost one whole floor of a building and may be hundreds of meter from the radar hardware.

g)
Ans:
No the FMS is not Connected to the avionics And is Used only for logistics Computerization a function

Really Perform on a laptop then the FMS is checking not embedded.

h)

Ans:-

Yes, both in the Simulation and in the thing being tested in the HIL Simulation Hardware is being Controlled on both side.

i)

Ans:-

Yes, in this case of System Combination and the Pace maker and the Person heart

j)

Ans:-

Yes, it is a Part of large System the engine & it is directly monitoring and controlling the engine through the Special hardware.

(1)2

A)

Ans:-

There are four main structural Components.

1) Central Processing Unit :-
Control the operation of the Computer & Perform its data Processing function often simply referred to as Processor

2) Main memory :-
Stores data.

3) I/O :-
Move data between the Computer and its external environment

4) System Interconnections :-
Some mechanism that Provides for Communication.

B)

Ans:-

The Characteristic of a family are as follows.

Similar or identical instruction set:
In some cases, the lower end of the family has an instruction set that is a subset of that of the top end of the family. this mean the program can moves up but not down.

Similar or identical operating system:
The same basic operation system is avialable for all family members.

Increase Speed:
The rate of instruction execution increase in going from lower to higher family members.

Increasing memory size:
The size main memory increase in going from lower to higher family member.

Increasing Cost:
At a given point in time, the cost of a system increase in a going from lower to higher family mem

C)

Ans:- A fundamental design approach first implemented in the IAS Computer is know as the Stored-Program Concept. this idea is usually attributed to the mathematician John von Neumann. The first Publication of the idea was in 1945.

D)

Ans:- The famous Moore's law, which was Profounded by Gordon Moore, Cofounder of Intel in 1965. Moore observed that the number of transistor that could be put on a single chip was doubling ever year. the pace slowed to be doubling every 18 month in the 1970 but has sustained that rate ever since.

Q. 3)

A)

Ans:- Computer Architecture refer to those

attributes of a system visible to a Programmer or, Put another way, those attributes that have direct impact on the logical execution of a Program.

Computer organization:
refers to the operational units & their interconnection that realize the architectural specification.

B)

Ans:

CISC:-
The current x86 offerings represent the result of decades of design effort on Complex instruction computer the x86 incorporates the sophisticated design principle once found only on mainframes and supercomputer & serves as an excellent.

RISC:-
The ARM architecture is used in a wide variety

of embedded System & is one of the most powerfull & best design Risc based System on the marked.

C)

Ans:

Microprocessors

micro processor chip include registers an ALU & some sort of control Unit or instruction Processing Unit logic.

Microcontrollers

A microcontroller is a single chip that contain the Processor, non volatile memory for the program (Rom) volatile memory for input & output (RAM) a clock and an I/O control Unit.

D)

Ans:

Cortex-A is

The Cortex-A and Cortex-A50 are application Processor intended for mobile device such as smartphone & e book readers.

Cortex-R:

The Cortex-R is designed to support real-time application in which the timing of events needs to be controlled with rapid response to events.

Cortex-M:

Cortex-M series processors have been developed primarily for the microcontroller domain where the need for fast, highly deterministic interrupt management is coupled with the desire for extremely low gate count & low possible power consumption

Q4
a
Ans:-

Here is a simple way to understand this problem.
Content are divided up into two 5 bit instruction. LH & RH
LH instruction = 01 0fA
OPCode = 01
address = 0fA
RH instruction = 21 0fB
OP code = 21

Since this is in hexadecimal form you have to converted the number to binary form.

LH instruction

01 = 0000001 = LOAD m(x)

m(x) refers to the memory address location 0FA

The first 5 bits of 08A should read - LOAD m(0FA)

RH Instruction.

21 = 0010000 1 = stor m(x)

m(x) refers to the memory address Location 0FB

The second 5 bit of 08A should read - stor m(0FB)

Finally the assembly language code for 08A 01 0FA 21 0FB is

LOAD m(0FA)

Stor m(0FB)

2) Here is a simple way to understand this problem.

Content are divided up into Two 5 bit instruction, LH & RH

LH instruction = 01 0FA

opcode = 01

address = 0FA

RH Instruction = 0F 0BD

OPcode = 0F

address = 08D
Since this is in hexadecimal from you have to converted the number of binary form.

LH instruction
01 = 0000001 = LOAD M(X)
M(X) refers to the memory address location 0FA
The first 5 address bits of 08B should read - LOAD M(0FA)
RH instruction
0F = 0000 1111 = jump + M(X, 0:19)
refer to the memory address location 08D
The second 5 bits of 08B should read - jump + M(08B, 0:19)
Finally the assembly language code for 08B 0FA of 08D is
LOAD + M(0FA)
jump + M(08D, 0:19)

3) Here is a simply way to understand this problem.
Content are divided up into two 5 bit instruction LH & RH
LH instruction = 02 0FA
opcode = 02

address = 0fA
RH instruction = 21 0fB
opcode = 21
address = 0fB
Since this is in hexadecimal from upto convert the number to binary from.
LH instruction
82 = 000010 = LOAD M(x)
M(x) refers to the memory address location 0fA.
The first 5 bits of 08C should read - LOAD M(0fA)
RH instruction.
21 = 010001 = stor M(x)
M(x) refers to the memory address location 0fB.
The second 5 bit of 08C should read - STOP M(0fB)
Finally the assembly address code for 08C 020fA 210fB.
is LOAD M(0fA)
STOR M(0fB)

b) Explain what is this program does?

Ans:-
In 08A address the M(0fA) transfer to the accumulator and

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take next instruction from left half of m(OBD).

2) In OBA address, the m(OFA) transfer to the accumulator & the transfer content of accumulator to memory location of B.