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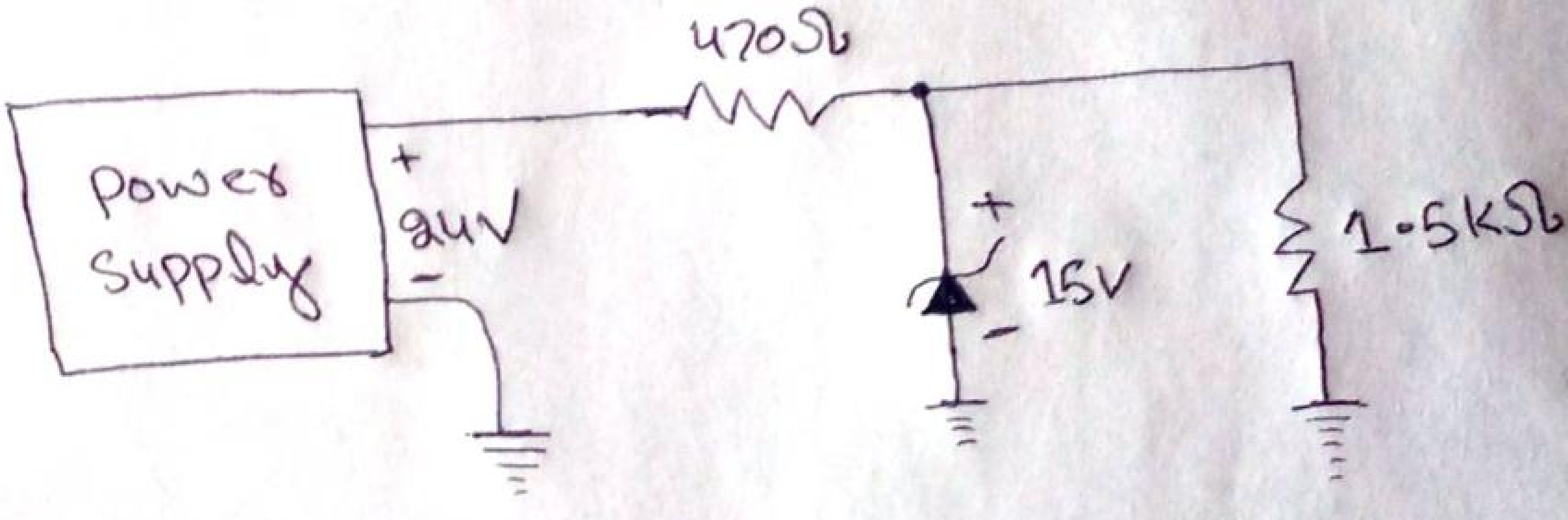
Dept: BS(CS)
(Final-Term)
paper: Basic electronics

-: Q1 :-
Part:-(a)

Answers:-



Given data:-

$V_s = 24V$

$V_Z = 15V$

$R_s = 470\Omega$

Solution:-

$$\text{Zener current} = \frac{(\text{Source voltage}) - (\text{Zener voltage})}{\text{Resistance}}$$

Putting values

$$\text{Zener current} = \frac{24V - 15V}{470\Omega}$$

$$\text{Zener current} = \frac{9V}{470\Omega}$$

Zener current = 0.019 A (or) 19 mA

-: Q1 :-

part: (b)

Answer:-

If The Zener diode is disconnected, the load voltage is in the form of Vth,

we know that;

$$V_{th} = \frac{R_L V_s}{R_s + R_L}$$

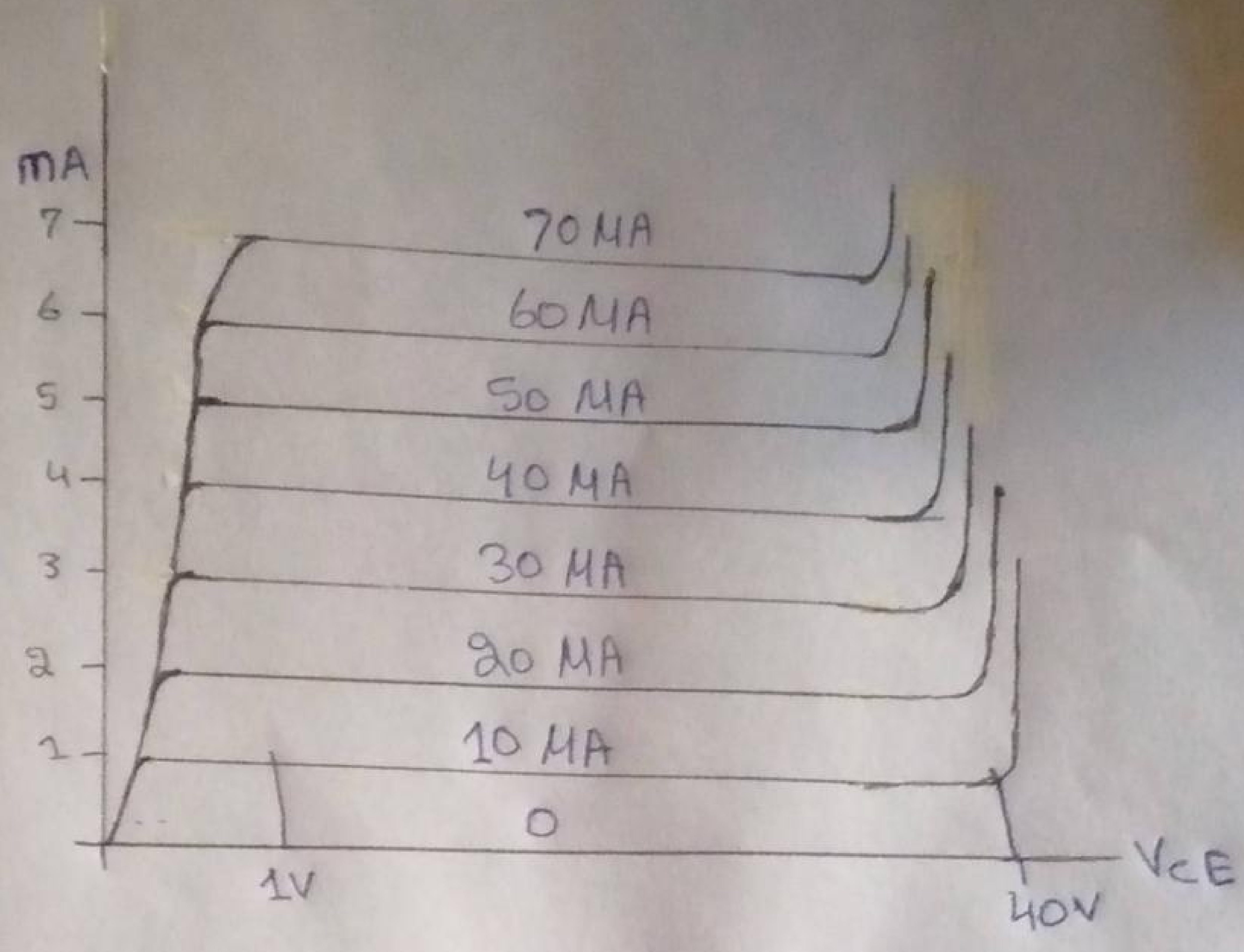
putting values in the formula

$$V_{th} = \frac{1.5k\Omega \times 24V}{470\Omega + 1.5k\Omega}$$

$$V_{th} = 18.27V$$

-: Q2 :-

Answers:- Set of Collector Curves



Operating Region of Transistor:-

(1) **Active Region:-**
Transistor operate in the active region when V_{CE} is between 1 & 40V.

(2) **Breakdown Region:-**
The transistor should never operate in this region because it will be destroyed.

(3) **Saturation Region:-**
Transistor operate in this region when V_{CE} is between 0V and a few tenths of a volt.

(4) **Cutoff Region:-**
Transistor operates in this region when base current is zero that we cannot see it. This small current is called Collector cutoff current.

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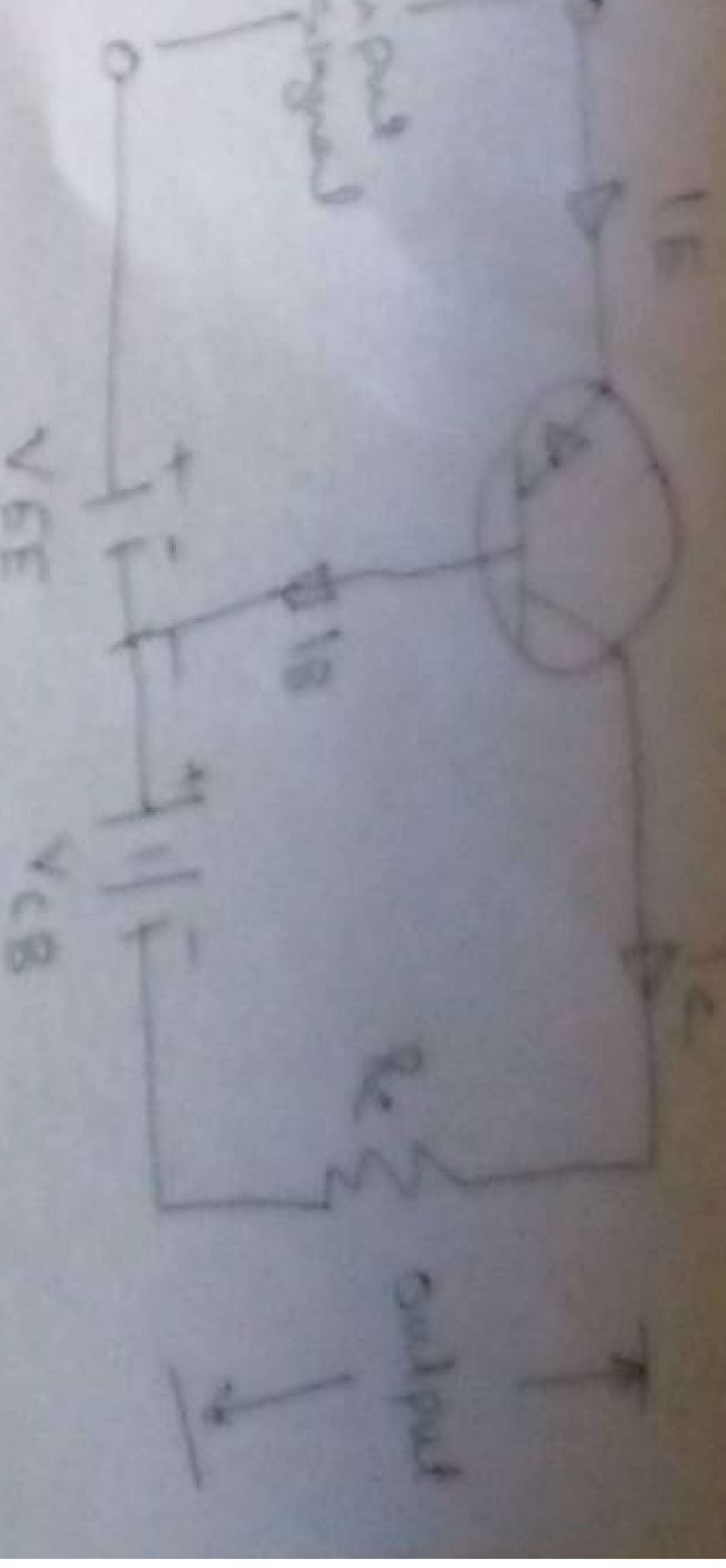
Answers:-

Common Base :-

In this Configuration we use base as Common terminal for both Input and output signals. The input is applied between the base and emitter terminal and the Corresponding output signal is taken between the base and collector terminals with the base grounded. Input parameter are VEB and IE & out parameter are VCB and IC. The Input current flowing into the emitter terminal must be higher than the base Current and collector current to operate the transistor, therefore the out Collector current is less than the input emitter current.

$$AV = \frac{Vout}{Vin} = \frac{(IC \times RL)}{(IE \times Rin)}$$



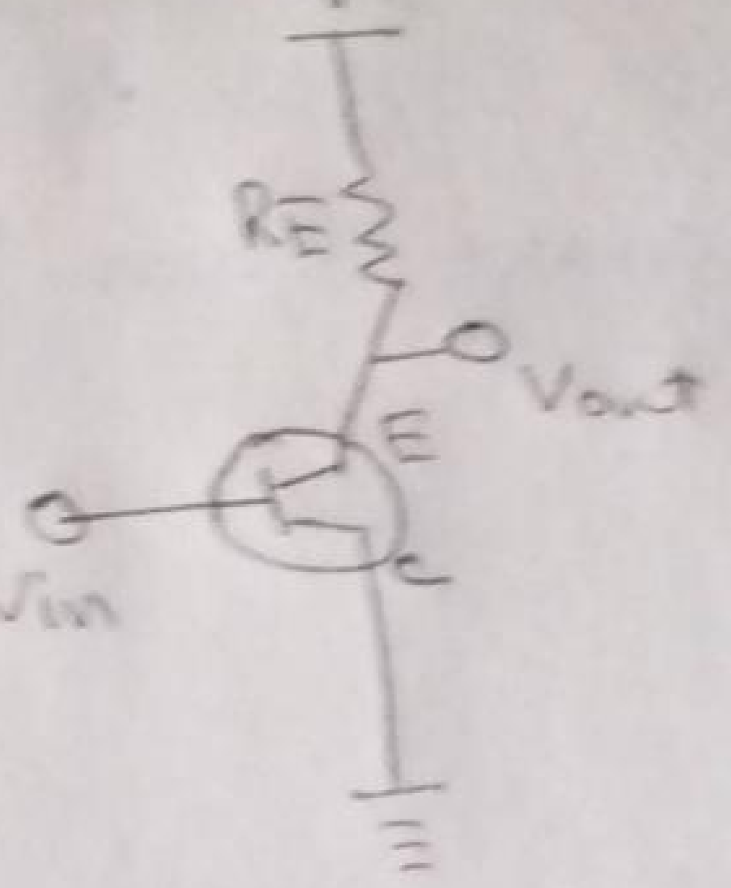
Current gain in common base Configuration is given as

α = output / input current

α = IC / IE

Common Collector :-

The common collector is another type of bipolar junction transistor (BJT) configuration where the input signal is applied to the base terminal and output signal taken from emitter terminal. thus the collector terminal is common to both the input and output circuits.



Common emitter :-

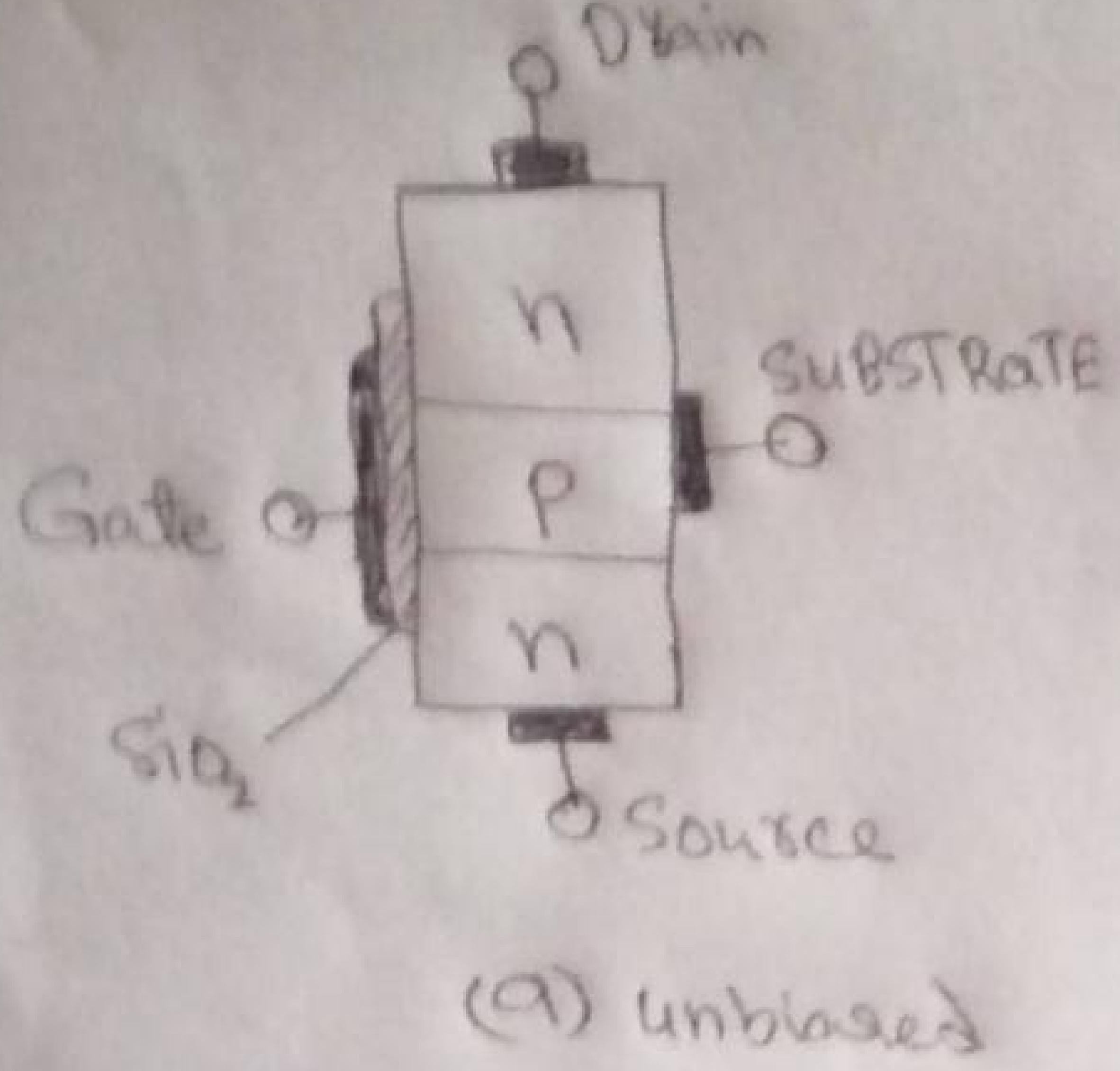
Common-emitter amplifier gives the amplifier an inverted output and can have a very high gain that may widely from one transistor to the next.

$$A_v \triangleq \frac{V_{out}}{V_{in}} = \frac{-g_m R_C}{g_m R_E + 1} \approx \frac{R_C}{R_E}.$$

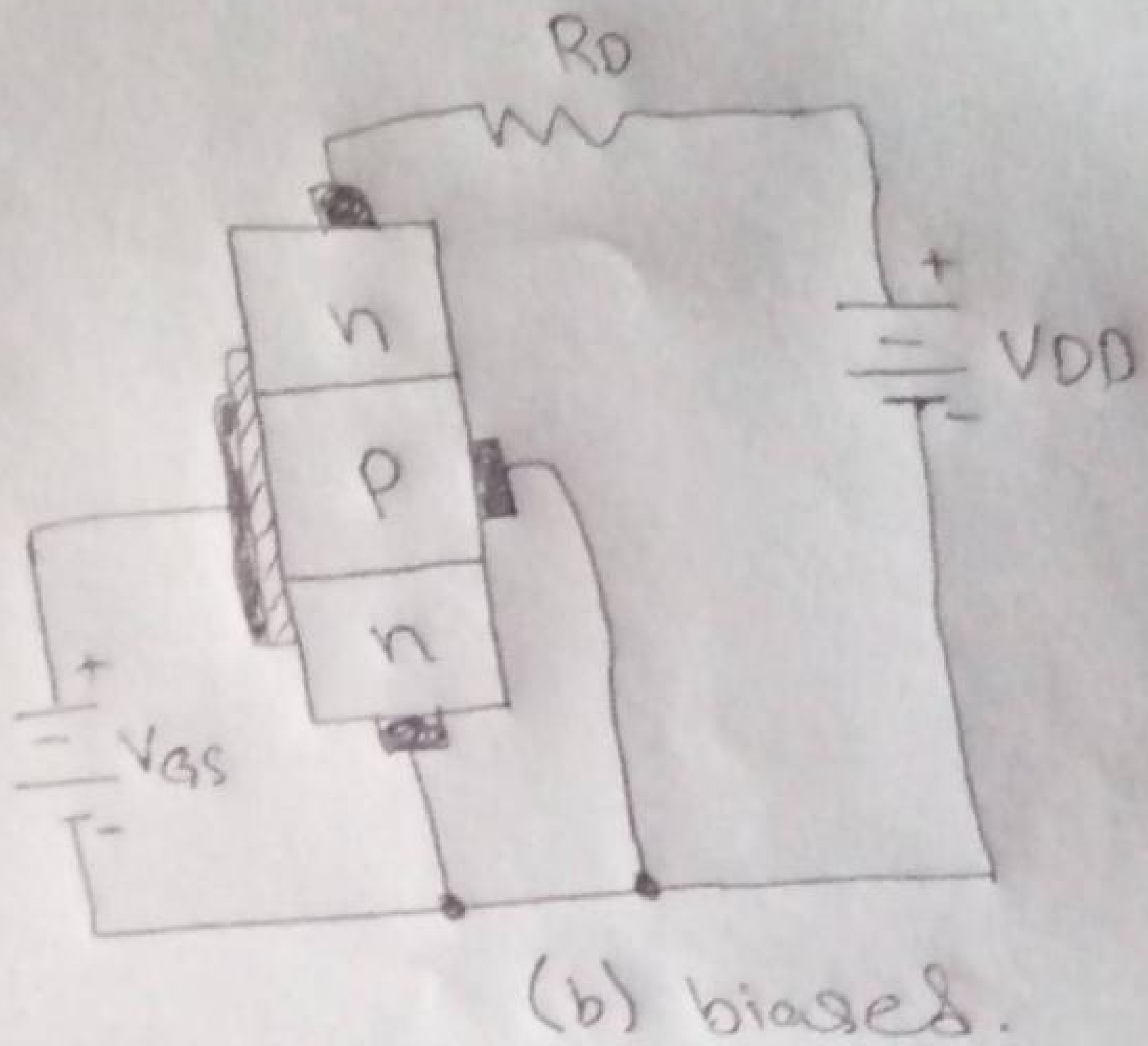
Answers:-

The Enhancement-Mode MOSFET:-

The depletion mode MOSFET was part to the evolution toward the enhancement-mode MOSFET abbreviated E-MOSFET.



(a) unbiased



(b) biased.

Explanation:-

E-MOSFET. The p substrate now extends all the way to the silicon dioxide. As you can see, There no longer is an n channel between the source and the drain. Figure (b) shows normal biasing polarities. when the gate voltage is zero, the current between source & drain is zero, For this reason an E-MOSFET is normally off when gate voltage is zero.

The only way to get current is with a positive gate voltage. when the gate is positive, It attract free electrons into the p region. The free electrons ~~begin~~ recombine with the holes next to the silicon dioxide. when the gate voltage is positive enough all the holes touching the silicon dioxide are filled and free electrons begin to flow from the Source to the drain The effect is the Same as creating athin layer of n-type material next to the silicon dixiode. This Thin Conducting layer is Called the n-type inversion layer. when it exits free electrons can flow easily from the Source to drain. The minimum VGS that creates the n-type inversion layer is called threshold voltage

The JFET is referred to as depletion-mode device because its conductivity depends on the action of depletion layers. The E-MOSFET is classified as enhancement-mode device because agate voltage greater than the theshold voltage enhances its conductivity. with zero gate voltage aJFET is on where as an E-MOSFET is off There fore, The E-MOSFET is considered to be a normally off device.

-: Q5 :-
Part (a)

Answers:-

Advantages & JFET:-

Following are the benefits of JFET:

- High input resistance
- Low noise figure.
- High efficiency as compare to BJT
- Operating frequency range is higher Compare to conventional BJT transistor.

Disadvantages of FET:

Following are disadvantages of FET:

- It has relatively lower gain-bandwidth product compare to BJT.
- Transconductance is low and hence Voltage gain is low.

Advantages of BJT:

1- The bipolar junction transistor (BJT) has large gain bandwidth.
2- The BJT shows better performance at high frequency.
3- The BJT has a better voltage gain
4- The BJT can be operated in low or high power applications.

5- The BJT has high current density.
6- There is low forward Voltage drop.

Disadvantages of BJT:

1- The bipolar junction transistor (BJT) more noise produced.
2- The BJT are more effect by radiation.
3- BJT has a low thermal stability.
4- The switching frequency of BJT is low.
5- It has a very complex base control so it may lead to confusion and reauires a skilful handing.

Comparison between BJT and FET:

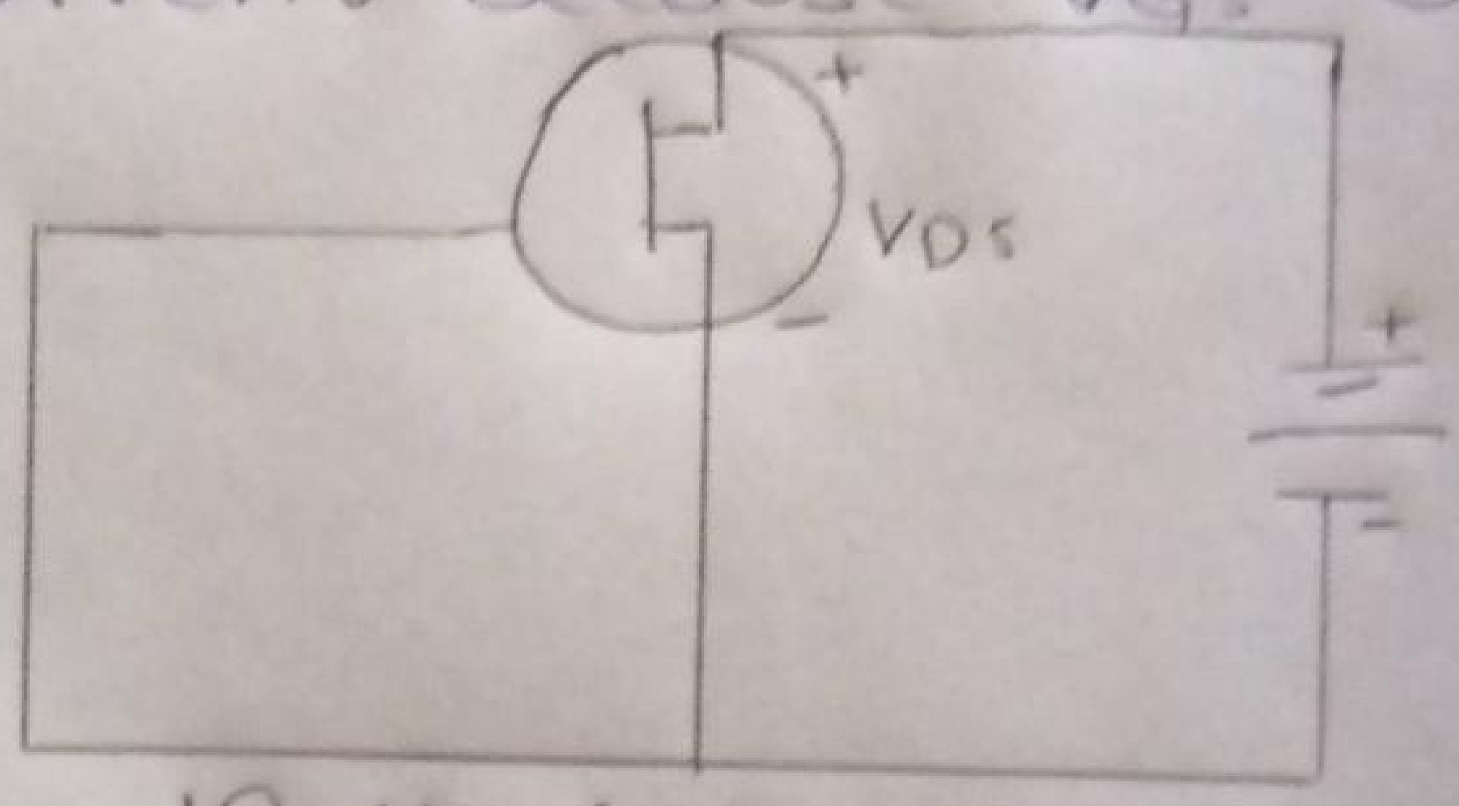
- Feild effect transistors are voltage Controlled.
- Bipolar junction transistors are current Controlled.
- In many applications FETs are used than bipolar junction transistors.
- The input impedence of feild effect transistors has high compared with bipolar junction transistors.
- Bipolar junction transistors are bipolar devices, in this transistor there is a flow of both majority & minority charge carriers.

-: Q8 :-
part(b)

Answers:-

<u>Drain Curves</u>:
JFET with normal baising voltages. In this circuit, the gate-source voltage V_{GS} equals the gate supply voltage V_{GG}, and the drain source voltage V_{DS} equals the drain supply voltage V_{DD}

<u>Maximum Drain current</u>:
If we short the gate to the source, as shown in Fig 13-4b we will get maximum drain current becouse $V_{GS} = 0$.



13-4 (b)

Why does the drain current become almost constant? when V_{DS} increases, the depletion layers expand when $V_{DS} = V_P$ the depletion layers are almost touching The narrow conducting channel therefore pinches off or prevents a further increase in current. This is why the current has an upper limit of I_{DSS}. The active region of a JFET is between V_P and $V_{P(max)}$ The minimum voltage

V_P is called the pinchoff voltage, and and the maximum voltage $V_{DS(max)}$ is the breakdown voltage. Between pinchoff and breakdown, the JFET acts like a current source of approximately I_{DSS} when $V_{GS} = 0$.

I_{DSS} stands for current drain to source with a shorted gate. This is the maximum drain current a JFET can produce. The data sheet of any JFET lists the value of I_{DSS}. This is one of the most important JFET quantities, and you should always look for it first because it is the upper limit, on the JFET current.