Name : irfan ullah

ID : 15431

LAB : no 11

Subject : Digital Logic Design

Course code(CS) : CSC-201

Program : BC (CS)

SYNCHRONOUS COUNTER

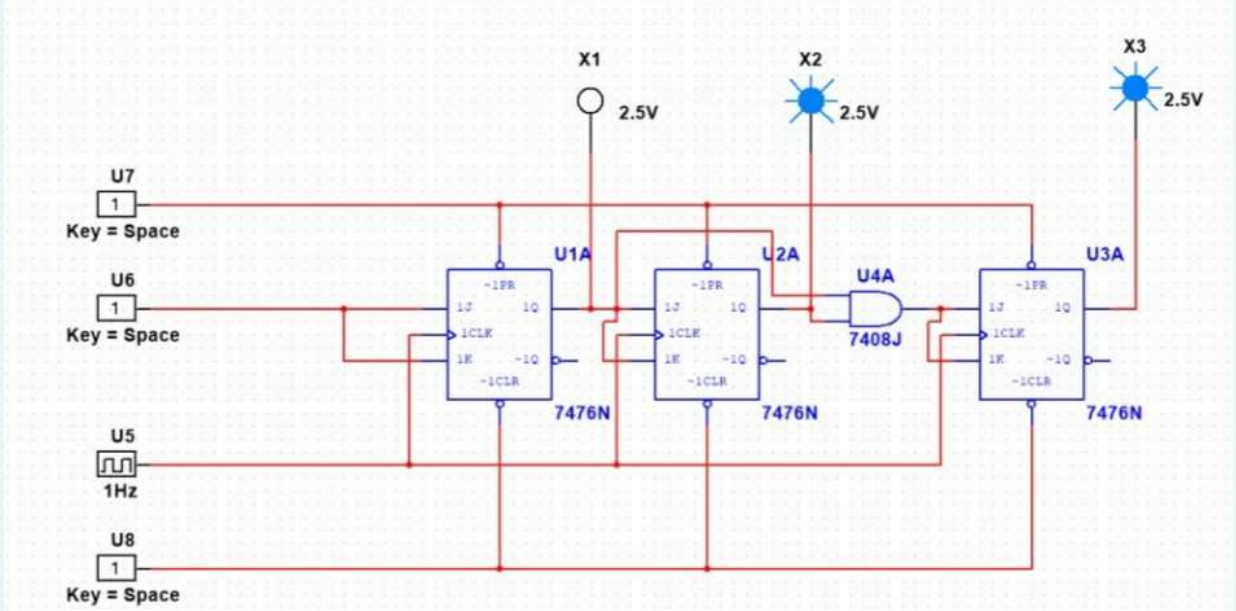
AIM:

Realization of 3-bit synchronous counter design.

PROCEDURE:

• Connections are made as per circuit diagram.

• Clock pulses are applied one by one at the clock I/P and the O/P is observed at QA, QB & QC for IC 7476.• Verify the Truth t



CLK	Q0	Q1	Q2
Initial	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (Recycles)	0	0	0

CONCLUSION:

o3-bit synchronous counter has been implemented and verified using ICs.