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Q No 2 :- (A)

Answer (A) :-

EEPROM	Flash memory
* EEPROM devices can erase any byte of memory at any time	* Flash memory can only erase an entire chunk, or "sector" of memory at a time
* EEPROM use NOR type memory.	* Flash memory uses NAND type memory.
* EEPROM is bytewise erasable	Flash is block-wise erasable

Q NO2:- part (B)

Answer (B):-

A Hard failure is a permanent physical defect so that the memory cells effected cannot reliably store data but become stuck at 0 or 1 or switch erractically b/w 0 and 1. Hard errors can be caused by harsh enviimmental abuse, manufacturing defects and wear.

where as

Softerror is a random, non destructive even that alters the Contents of one or memory cells without damaging the memory. Soft errors can be caused by power supply problems or alpha particles.

Q NO3:- (f) part.

Answer (f):-

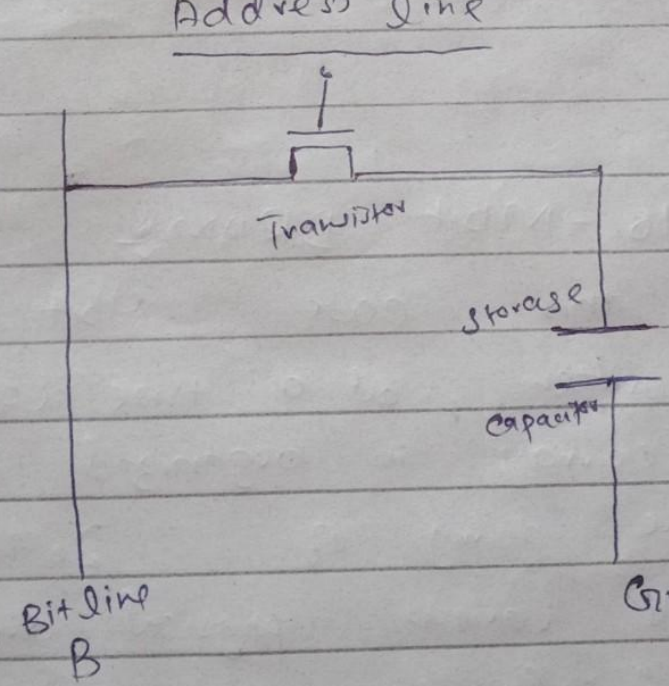
CD Read operation:-

when the address line is selected, the transister

turn on and the charge stored on the capacitor is leg out on to a bit line and to a sense amplifier it compares the capacitor voltage to a reference value and determine if the cell contain a logic 1 or logic 0.

* Write Operation:

A voltage signal is applied to a bit line a high voltage represents 1 and a low represents 0.



Q) No 1:- (C)

Ans (C) &

Read operation as

In SRAM for any operation to be performed. The word line should be high To perform read operation initially

write operation is Cosider the memory bit consists of Q=0 and Q' = 1.

Q) No 1 (D) &

Answer (D) &

16 - Mbit DRAM &

In this case 4bit are read or written at a time Logically the memory carray is organized as four square carry of 2048 by 2048 elements various physical awarse meant are possible. In any case the elements of the array are connected by both horizentel line comect by

both horizontal to the select Terminal of each cell in its row each vertical line connect to the Data in/ save Terminal of each cell is column. Because any Ubits are ready/written to this dram. there must be multiple DRAM connected to the memory controller to read/write a word of data to the bus.

Q NO 1 (e):-

Answer (e) :- The DVD's greater capacity is due to three differences from CD's.

(1) Bits are passed more closely on a DVD. The spacing b/w loops of a spiral on a CD is 1.6 μm and the maximum distance b/w pits along the spiral is 0.834 μm.

(2) The DVD employs a second layer of pits and lands on top of the first layer. dual layer and by adjusting focus. The lasers in DVD drives can read each layer separately.

(8) The DVD-ROM can be Two sided whereas dates are recorded on only one side of a CD. This brings Total capacity upto 17GB.

Q NO 28 (D) part

Ans (D) &

parallel access and independent access RAID schemes?

(1) Parallel access?

All member disk participate in the execution of every I/O request. Typically the spindles of the individual drives are synchronized so that each disk head in the same position on each disk at any given time.

(2) Independent access?

Each member disk operates independently, so that separate I/O requests can be satisfied in parallel.

Q NO 2:- (C)

Ans (C) &

Disk read/write heads are the small part of disk drive which move above the disk platter and transform the platters magnetic field into electrical current (read the disk) or, vice versa, transform electrical current into magnetic field (write the disk).

Q NO3(A) part &

Answer (A) &

Memory Access Methods:-

There are 4 types of memory access method.

1) Sequential Access:-

In this method the memory is accessed in a specific linear sequential manner, like accessing in a single linked list. The access time depends on the location

of the data. Applications of this sequential memory access are magnetic tapes, magnetic disk and optical memories.

(2):- Random Accessi-

In this method, any location of the memory can be accessed randomly like accessing in Array physical locations are independent in this access method.

Application of this random memory access are RAM and ROM.

3) Direct Access

In this method, the particular location of the memory can be accessed directly like accessing in Array. This method is a combination of above two access methods. The access time depends on both the memory organization and characteristics of storage technology. The access is semi-random or direct.

Application of thus direct memory access is magnetic hard disk read/write heads.

4)& Associate Access&

In this memory, a word is accessed rather than its address. This access access method is a special type of random access method. Application of thus direct memory access is Cache memory.

Q NO3 (b) part

Answer (B)&

Principle of locality&

The principle of locality states that data in the vicinity of a referenced word are likely to be referenced in the near future.

Q NO(3) (c)

Ans (c)&

Possible approaches of cache coherency&

Possible approaches to cache coherency include the following

Bus watching with write through&

Each cache

Controller monitors the address lines to detect write operations to memory by other bus masters. If another master writes to a location in shared memory that also resides in the cache memory the cache controller invalidates that cache entry this strategy depends on the use of a write though policy by all cache controllers

* Hardware Transparency:

Additional hardware is used to ensure that all updates to main memory via cache are reflected in all caches. Thus, if one processor modifies a word in its cache, this update is written to main memory. In addition any matching words in other caches are similarly updated.

* Non-cacheable memory:

Only a portion of main memory is shared by more than one processor, and this is designed as non-cacheable. In such a system, all accesses to shared memory are cache

misses, because the shared memory is never copied into the cache. The non-cacheable memory can be identified using chip-select logic or address bits.

(3)

(1) NO (D)

Answer (D)

There are two practical issues peculiar to SSDs that are not faced by HDDs:

- SDD performance has a tendency to slow down as the device is used.
- The entire block must be read from the flash memory and placed in a RAM buffer.
- The entire block from the buffer is now written back to the flash memory.
- Flash memory becomes unusable after a certain number of writes
- Techniques for prolonging life.
- Front endings the flash with a cache to delay and group write operations.
- Using wear-leveling algorithms that evenly

distribute writes accross block of cells.

- Bad-Block management techniques.
- Most flash devices estimate their own remaining lifetimes so systems can anticipate failure and take preemptive action

Q.No 1 part (A)

Ans:-(A) Words

The natural unit of organization of memory. The size of a word is typically equal to the number of bits used to represent an integer and to the instruction length.

- Addressable unit

On some systems, the addressable unit is the word. However, many systems follow addressing at the byte level. In case, $\partial A = N$.

- Unit of Transfer

For main memory, this is the number of bits read out of or written into memory at a time. The unit of transfer need not equal a word or an addressable unit.

Q) Ans(4) & (a) part

Answer: (A)

Least frequent recently used (LFRU) :

The least frequent recently used (LFRU) [11] cache replacement scheme combines the benefits of LFU and LRU schemes LFRU is suitable for 'in network' cache applications, such as information centric networking (ICN). Content Delivery networks (CDNs) and distributed networks in general. In LFRU, the cache is divided into two partitions called privileged and unprivileged partitions. The privileged partition can be defined as a protected partition. if content is highly popular, it is pushed into the privileged partition is done as follows: LFRU evicts content from the unprivileged partition, pushes content from privileged partition, to unprivileged partition, and finally inserts new contents into the privileged partition. In the above procedure the LRU is used for the privileged partition and an approximated LFU (ALFU) scheme is used for the unprivileged

partition, hence the abbreviation LFRU.
The bask idea is to filter out the locally popular moments with AIFU scheme and push the popular contents to one of the privileged partitio.

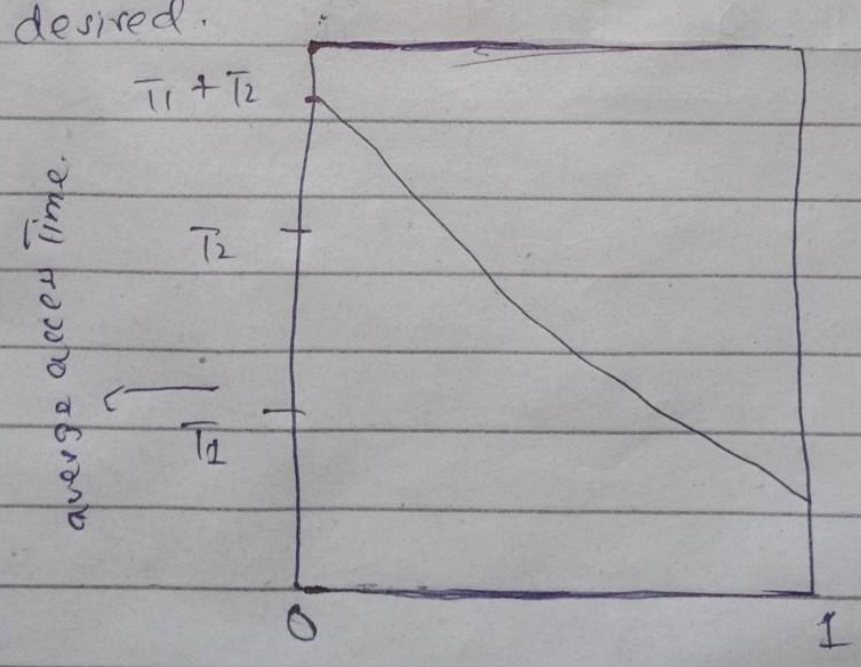
Q NO(4) (a) part.

Answer (a) :-

In our example, suppose 95% of the memory accesses are found in Level 1. Then the average time to access a word can be expressed as.

$(0.95)(0.01\mu s) + (0.05)(0.01\mu s) = 0.0095 + 0.0055$
$= 0.015\mu s.$

The average access time is much closer to $0.01\mu s$ than to $0.1\mu s$, as desired.



(Q NO 4:-(B)

Answer (B)

Total block in the cache

$= 8\text{k bytes} / 16\text{ bytes} = 2^3 \times 2^{10} / 2^4 = 2^9 = 512$

Number of set = number of block in cache/2.

Number of set = 512/2

Number of set in cache = 256

Number of set in cache $= 2^8$

Number of set = 8

Size block = $16 = 2^4$

Size of memory $= 2^6 \times 2^{20} = 2^{26}$

Tag = size of memory - set - size of block.

Tag = 26 - 8 - 4

Tag = 14

Tag	set	Size of block
14	8	4

Q NO 4 (c) part :-

Ans (c) :-

$$M = 8$$

$$2^k - 1 >= k + m$$

$$2^4 - 1 >= 4 + 8$$

$$15 >= 12$$

1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	1	1	0	0	1	0	0	1	0

The check bits are in a bit number 1, 2, 4, 8. check bit 8 calculated by values in bit numbers 9, 10, 11, and 12.

check bit 4 calculated by values in bit number : 5, 6, 7 and 12.

check bit 2 calculated by values in bit numbers : 3, 6, 7, 10 and 11.

check bit 1 calculated by values in Bit number : 3, 5, 7, 9, 10 and 11.

The, check bits are : 1011.

Q NO4 (D) part 8

Ans8

So,

7200 evaluation in 60sec.

1 revolution in 60/7200

1 revolution in 6ms.

1 revolution = covering one entire track = 500 sector

500 sector = 6ms

1 sector = 8 microsecond.

Now there are 2 different things

① 2500 sectors So time = 2500 × 8ms = 20ms.

② 1.28MB = 1342177.28 Bytes or 2621.44 sectors = 2622 sectors = 20.976 ms

Total Time case :-

Case ① 4+2+20 = 26ms

case ② 4+2+20.976 = 26.976ms.