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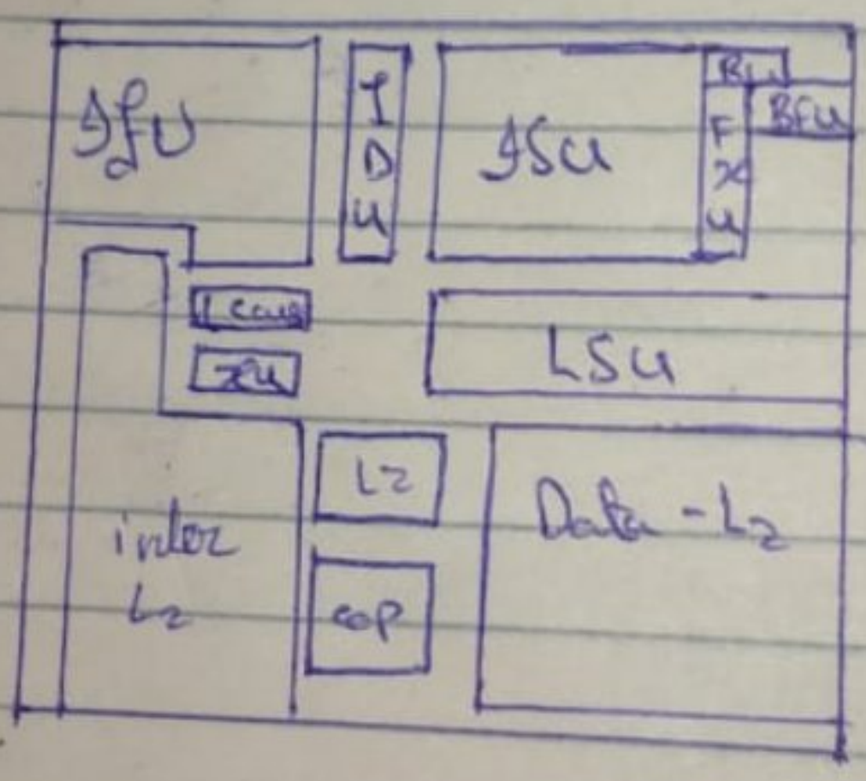
Computer Architecture

Give ans to each of the following.

Q-NO-(1)

Ans (1)



* IDU stand for instruction decode Unit. The IDU is responsible for the parsing and decoding of all z/Architecture operation codes.

* LSU:- stand for load store Unit it is responsible for handling all type of operand access of length modes and formates.

* TLB: Stands for Translation Unit. This unit translate logical address from instruction into

physical address in the main memory.

* FXU :- The fxu excutes fixed point arithmetic operation.

* BFU :- Stands for Binary Floating Point Unit the BFU handles all binary and hexadecimal floating point operation

* DFU :- Stands for Decimal floating point unit the DFU handle both fixed point and floating operation as numbers that are stand as decimal digits.

* RU :- (Recovery Unit). The RU keeps a copy of the complete state of the system that include all registers.

* CP :- (Dedicated Co-processor) The CP is responsible for data compression and function for Each other.

* L_2- Caches :- This is control logic that manage the traffic through the two L_2-caches.

* Both L_2 :- MBS, L_2 cache for all memory traffic other than instruction.

* Instr L_2 :- INS instruction code.

Ans(B) :- The IAs operations by respectively performing an instruction cycle. Each instruction cycle consists of two sub-cycle.

1) Fetch cycle :- The opcode of next instruction is called into the UR and the address portion is loaded into the MAR. This instruction taken from the IBR.

2) Excute Cycle :- This control circuicy interprets the opcode & execute the instruction by sending out the appropriate control and signal to cause data to be moved or an operation to be performed by Icu.

Ans(C) :- Often embeded system are tightly coupled to their enviroment. This can give rise to real time contraints such as required speeds of motion. This imposes more complex real time constants list of daily life.

Ans(D) :- The given below are the application that require the great power of contemporary microprocessor system are 1) Image Processing 2) Three dimension 3) Speach recognizing 4) Undo conferencing 5) Multimedia authoring 6) Voice and video construction of files 7) Simulator modeling.

Ans (E) :- Here some of techniques used to increase the speed.

① pipelining :- pipelining enable to processor to work simultanisly on multiple instruction by performing a difficult phase for each of the multiple instruction.

② Branch prediction :- Branch prediction. potentially increase the amount of work awaible for the processor to execute.

③ Superscalar Execution :- This is the activity to issue more than one instructions in every processor clock cycle.

Ans (F) The process which is created due to increase the clock speed and logic density of the processor are given below.

* Powers :- As the density of logics and the clocks speed on a chip increase so the power density increase and also dissipated that heat.

* Memory latency :- Memory access speed (latency) and transfer speed (through put) by processor speed.

Ans (G) The speed using a parallel processor with N processor that fully exploits the parallel portion of

the program is as follows:

Speedup time 1x executes program on a single processor / time to executes program on N parallel processor =

$$T(1-f) + Tf/T(1-f) + Tf/N = K(1-f) + f/N$$

Ans (H)* Multicore : The use of multicore processor on the same chip provides the potential to increase performance without increasing the clock rate.

* MIC : leap in performance as well as the challanges number of core.

* Cplls : Core designed to perform parallel operation on graphics. It is used to encode and readed 2D and 3D as well as process video.

Ans (4) QPI protocol layer :

In this layer of transfer. One key function perform at this level in a cache coherency protocol, which deals with making sure that main memory values held in multiple caches are consistent. A typical data packet payload is a block of data being sent to or from a caches.

Ans (d) Physical and logical Architecture.

* A sof complex device also refered to as a chipct or a host bridge connect the processo and memory subsystem to the PCI Express Switch fabrics comprising one or more pcie and pcie Switch devices.
* Pcie links from the chipset may attach to the following kind of devices that implements Pcie.
* Switch : The Switch manages multiple pcie streams
* Pcie endpoints : An I/O devices or controllers that implement Pcie Such as eligibit ethernet Switch a graphics or video controllers clock interface or a communication controller.
* Pcie/Pci bridge : Allows older Pci devices to be connected to Pcie-based Systems.

Q-NO-2

Ans (a)

Main structured Component of a Computer -

There are four main structured component.

1) CPU :- Controls the operations of computer and perform its data processing function ; often simply refessed to as processor.
2) Main memory : Stores codes
3) I/O : Moves data b/w the computer and extend environments.
4) System interconnections as some mechanism that provides for communiction.

Ans (b) The characteristic of a family are as follow

* Similar or identical instruction set o In some cases the lower end of family has an instruction set that is a subset of that of the top of the family. This means that program can move but not down.

* Similar are identical operating system o The same basic operating system is availble for all family
* Increasing Speed :- The rate of instruction execution increasing in going from lower to higher family members.

Ans (c) :- Stored Program Computer.

A fundamental design approch first implemented in the IAS compter is kenown as the stored program concepts. This ideas is usually attributed to the mathematics John von Neumann. The first publication of the idea was in 1945 proposed by von Neuman for a new Computer the EDVAC in 1946, Von Neuman and his colleques begain of a new stored program computer.

Ans (a) Moore's Law :-

The famous Moore's law which was proposed by Gordon Moore cofounder of intel in 1965. [Moor 65]. Moore observed the number of transistor that could be put on a single chips was doubling every years 18 months in the 1970s but has sustained by that rated ever since.

Moore's Law are pretend.

1) The lost of computer logic and memory circuitry has fallen at a dramatic rate.
2) Because logic and memory elements are placed closer together on more density packed chips. The electrical path length is shorted increasing operating.
3) The computer becomes smaller making more convenicied to place in a variety
4) There is a reduction in power requirment
5) With more circuitry on each chip, there are fewer interchip connections.

Ans (b) Instruction Cycle state Diagram :-

- Instruction address calculation.
- * Instruction Petch
- * Instruction operation decoding
- * Operand address calcution
- * Operand fetch
- * Data operation
- * Operand store.

Ans (F) Classes :-

(i) Program :-
It is generated by some condition that occurs as a result of instruction execution.

(ii) Timer :-
It is generated by some conditions occurs as a result of instruction, execution

(iii) I/O :-
It is generated by an I/O controller

(iv) Hardware failure :-
It is generated by a failure or memory parity errors.

Ans (G) Bus Interconnection Scheme :-
The most computer interconnections structure are based on the use of one or more system buses.
A system bus consist, typically from about fifty to hundred of separate lines. The lines can be classified into three functional groups.
Data Address & control lines.

Q-No-3

Differentiate each of the following

(a) Computer Architecture

(i) Architecture what the computer does
(ii) Computer Architecture deals with function
(iii) Behaviour of computer system
(iv) Architecture indicates us hardware

Computer Organization :-

(i) Organization describe how it does it
(ii) Computer organization deals with structral relationship
(iii) Organization indicates its performace.

Ans (b) :- RISC

(i) The original microprocessor GSA
(ii) Instructions can take several clock cycles
(iii) More efficient use of RAM
(iv) large number instruction
(v) Compound Addressing modes

CISC :-

(i) Redesigned GSA that emerge in the early 1980s
(ii) Single cycle instructions
(iii) Heavy use of RAM

(N) Small number of fixed-length instructions
(J) limited addressing modes.

Ans (c)

Microprocessor :-

(i) Microprocessor is a heart of computer system
(ii) Since memory and I/O has to be connected externally the circuit becomes large.
(iii) Cost of the entire system increases.
(iv) Mainly used in personal computer.

Microcontroller :-

(i) Micro controller is a heart of embedded system
(ii) Since memory and I/O present internally, the circuit is small
(iii) Cost of the entire system is low
(iv) Used in washing machine, MP3 players.

Ans (d)

Architecture profile	Cortex-A	Cortex-R	Cortex-M
	ARMv7-A	ARMv7-R	ARMv7-M
	ARMv8-A	ARMv8-R	ARMv8-M
Instruction set	32-bit/64bit	32-bit	32-bit
Interrupts	Software manage	Deterministic software manage	Hardware manage
Operating System support	Rich OS/RTOS	RTOS	RTOS
Example processors	Cortex-A1	Cortex-R8	Cortex-M7

Ans (e)

Interrupt

* In the interrupt cycle the processor check to see if anyone interrupts have occured, indicate by the presence of an interrupt signal.

Without Interrupt :-

* If no interrupts are pending, the processor proceeds to the fetch cycle and fetches next instruction of current program.

Ans (f)

Disable interrupt :-

Simply means that the processor can and will ignore that interrupt request signal. if a interrupt occurs during this time, it generally remains pending and will be checked by the processor after the processor has enabled interrupts.

Nested Interrupt :-

is to allow an interrupt of higher priority to cause a lower-priority interrupt handler - to be it-self interrupted. A user program beings at t=0 at t=10 - printer interrupts occurs.

Ans (C)* Programming in Hardware:- Suppose we contract a general purpose configuration of arithematic and large function - This of Hardware used perform various function data in the orignal case.

* Programming in Software:-

(The new Method programming is much easier instead of rewriting the hardware for each new program. All new need to do is provide a new sequence of code. Each code is an effect can instruction and part of the hardware interpt exact interaction and generates control signal.

(2)

Q-NO-4

Ans (A)(i) LH instruction = 01OFA
Solution OP code = OFA
RH Instruction = 210FB
OP code = 21
address = 0FB

This is a hexadecimal form you have to convert the numbers to binary form (use IAS instruction set)
LH instruction.
01 = 00000001 = Load M(x)

M(x) refers to memory address location OFA
The first 5 bits of OBA should read.
Load - M(OFA)

RH Instruction
H :0010000] = S10eM(x)
M(x) refers to the memory
address location OFB
The second 5bit of OBA should read STOR M(OFB)
finally the assembly language code for OBA
of OFA210FB is

LOAD M(OFA)
STOR M(OFB)

② Contents are divided up into two 5 bit instructions . LH & RH

LH Instruction = 01OFA
OP code = 01
address = OFA

RH Instruction = 0F08D
OPcode = OF
address = 08D

This Hexadecimal form covert into binary form

LH instruction &
01 = 0000001] = LOAD M(x)

M(x) refers to the memory address location OFA
The first 5 bit of 08B should load M(OFA)

RH Instruction :-
DF = 00001111 = jump to M(x, 0:19)
refers to the memory address 08D
Finally the assembly language code for
08B 01 0FA CF 08D is
Load M(0FA)
Jump + M(08D, 0:19)

(3.) LH instruction = 020FA
OP code = 02
address = 0FA

RH instruction = 210FB
OP code = 21
address = 0FB

(b:) What is Program does :-
Ans: In 08A address the M(0FA) transfer to the accumulator to the memory location 0FB.
In 08B address the M(0FA) transfer to the accumulator from left half of M(08D)
In 08C address the M(0FA) transfer Accumulator and transfer contents to memory location (0FB)

Part - B

Answer :-

(a) Opcode = 00000001

operand = 0000000000001010

(b) In the beginning, the CPU have to fetch the instruction from the memory, then the instruction will include the address of the data which is required to load. Through the execution time, the memory will be accessed in fet time to load, the data contents which is loaded at that address for a total of two trips to memory

PART - C

Effective CPI :-

CPI = (1 x 450000) + (2 x 320000) + (2 x 160000) + (2 x 50000) / 100

CPI = 1620000 / 100

CPI = 1620

MIPS :-

MIPS rate = 60 MHz / 1620 x 10^6

MIPS rate = 60 x 10^6 Hz / 1620 x 10^6

MIPS rate = 60 Hz / 1620

MIPS rate = 0.037

Execution Time :-

T = Ic / (MIPS x 10^6)

T = 104000 / (0.037 x 10^6)

$\bar{I} = 2811 \times 10^{-3}$

$T = 2.811$ Sec

PART - D

Solution :-

(a)

Instruction type	CPI	Instruction time
Arithmetic logic	1	60%
load/store with cache	2	18%
Branch	4	12%
Memory reference with cache miss	12	10%

The average CPI $= (1 \times 0.6) + (2 \times 0.18) + (4 \times 0.12) + (12 \times 01) = 2.64$

Therefore CPI has been increased since the time for memory access is also increased.

(b) MIPS $= 400/2.64 = 152$

There is corresponding drop in the MIPS rate.

(c) $T = Ic / MIPS \times 10^6)$

for the one processor

$T_1 = (2 \times 10_6) / (178 \times 10_6) = 1$ ms

for the 8 processor each program processor execute 1/8 of the 2 million

(d) By depending on the information given, it is not obvious how to quantify the effect in Amdahl's equation. Therefore if it is supposed that the fraction of code.

PART : E

1(a) The PC contain 300, the address of the first instruction. This value is loaded into the MAR.

(b) The value in location 300, is loaded into MBR and the PC is incremented. The two steps can be done in parallel.

(c) The value in the MBR is loaded into the IR

2(a): The address portion of the IR (940) is loaded into the MAR.

(b): The value in location 940 is loaded into the MBR

(c): The value in the MBR is loaded into the AC.

3(a) The value in the PC (302) is loaded into MBR and PC is incremented

(c) The value in MBR is loaded into the IR

PART - F

Answer :-

a) 224 = 16 MBytes

b)i) If the load address is 32 bit the whole address can be transfer at once and decoded in memory, However the data bus in only 16 bits. It will requires 2 cycle 1: fetch 0

ii) The 16 bits of the address placed on the address bus can't access whole memory interface control is needed to latch the first of the address & then the second part.

c) The program counter must be atleast 34 bits, Typically 32-bit microprocessor will have a 32bit external address bus and 32 bit program

PART G

A bus cycle takes 0.25 MHz, So a memory cycle takes 1us. If both operands are even aligned it takes 2 cycles to fetch the two operands. If one is odd aligned the time required is 3us. If both are odd aligned, the time required is 4us.