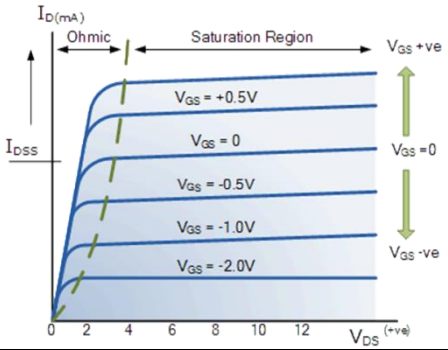
Department of Electrical Engineering
Assignment
Date: 14/04/2020

Course Details

Course Title: Electronic Circuit Design **Module:** 04
Instructor: **Total Marks:** 30

Student Details

Name: syed M zahoor **Student ID:** 12595

Q1.	(a)	**Explain** the drain characteristic curve of D-MOSFET given below.  	Marks 07 CLO 1
	(b)	**Sketch** the hybrid model and write equations for the transistor in common emitter configuration.	Marks 06 CLO 1
Q2.		A certain operational amplifier has a common mode gain of 0.6 and an open loop differential voltage gain of 400,000. **Evaluate** the CMRR & express it in decibels.	Marks 05 CLO 2
Q3.	(a)	**Explain** the concept behind negative feedback in operational amplifiers.	Marks 06 CLO 2
	(b)	**State** the following statement as **True** or **False** and also give the reason for your answer: "The output of a summing amplifier is positive"	Marks 06 CLO 2

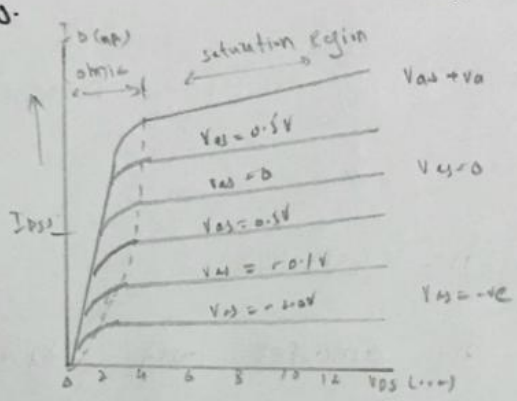
Electronic Circuit Design

Name :- Syed. Muhammad. Zahoor

Student ID :- 12595

Q②

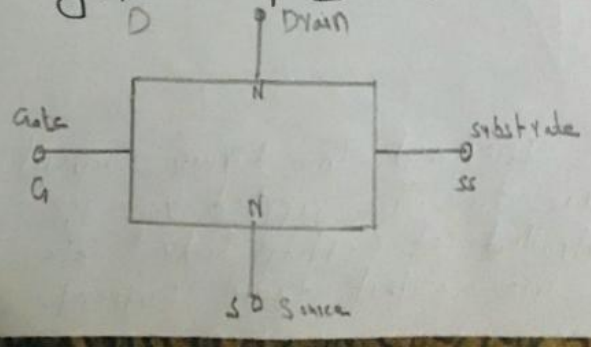
(a) Explain The drain characteristic curve of D-Mosfet given below.

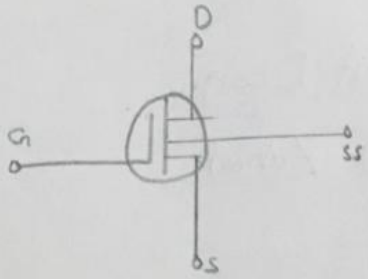


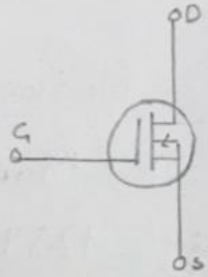
Ans D-MOSFET:-

A D-Mosfet is a deplition mosfet mean that the Threshold voltage is negative Instead of positive and its also called a normally on Mosfet because it is on at a gate Source of Zero voltage.

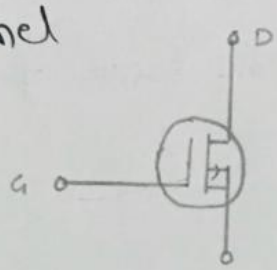
Schematic Symbols of D-Mosfet:







N- channel

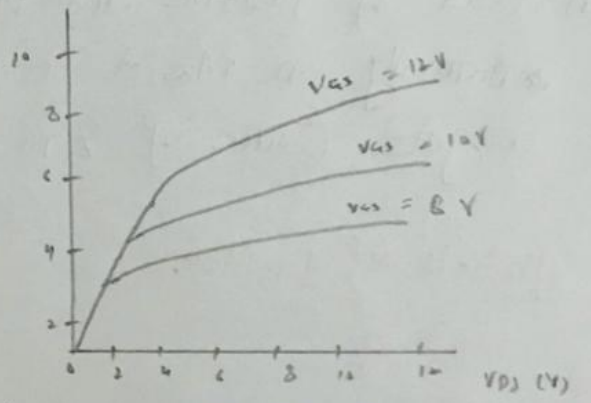


P- channel

Drain characteristic curves

The mosfet and drawn blw

The Drain Io and The ~~blw~~ Source voltage V_{DS} The Characteristic Curve shown below for different Inputs.



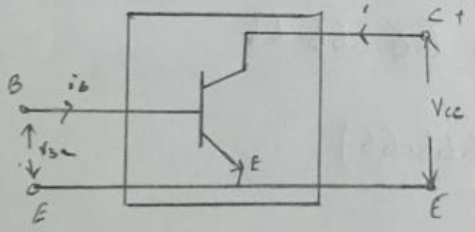
When V_{DS} is Increased The Drain Current I_D Should Increase but due to The applied V_{GS} The drain Current I_D controlled at certain level Hence The gate Current controls the output drain Current.

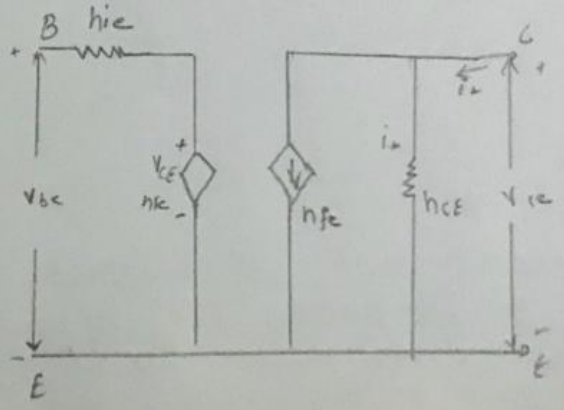
Q1 (b) Sketch the hybrid model and write equations for the transistor in common emitter configuration

Ans:- In the common emitter of the configuration the Input Signal is applied between the base and emitter terminals of the ~~transf~~ transistor and the output apears b/w the collector and emitter terminals. The Input voltage (V_{be}) and the output current (i_e) are given by the following eqn.

$$V_{be} = h_{ie} \cdot i_b + h_{re} \cdot V_c$$
$$i_e = h_{fe} \cdot i_b + h_{oe} \cdot V_c$$

Configuration:-





Q(2)

Given :-

A_{OL} = open loop differential voltage gain

= 400,000

common mode gain = A_{cm} = 0.6

Find :-

CMRR = ?

Solution

We know that

$$CMRR = 20\log\left(\frac{A_{OL}}{A_{cm}}\right)$$

$$= \frac{A_{OL}}{A_{cm}} = \frac{40,000}{0.6}$$

$$= 66,666.66$$

$$= 20\log(66666.66)$$

CMRR = 94.47 dB Ans

Q6
(A) Explain The concept behind negative feedback In operational amplifiers.

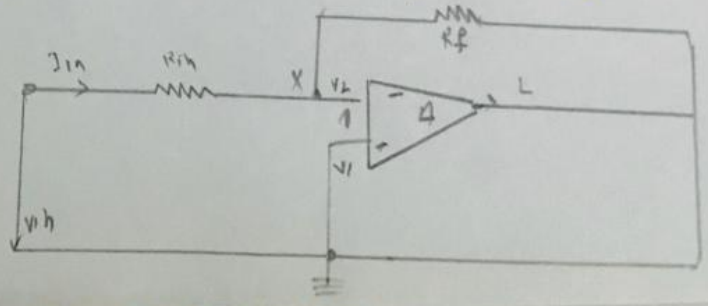
Ans:-

Negative feedback:-

It is The process where by a portion of The output voltage of an amplifier is returned to The Input with with a phase angle that opposes (or Subtract from) The Input Signal.

concept behind The negative feedback:-

Negative feedback is The process of feedback a fraction of The output Signal back to The Input but to make The feedback negative we must feed it back to negative or Inverting output terminal of The op-amp using an external feedback ~~connection~~ resistor called Rf. This feedback connection b/w The output and The Inverting input terminal force The differential Input voltage toward Zero.



(Q3)

⑤ State the following Statement as True or false also given the reason for your answer:
"The output of a Summing amplifier is positive"

Ans:-

The Summing Amplifier is another type of operational amplifier circuit configuration that is used to combine the voltage present on two or more Input into a Single output voltage. The Statement is false because when the Summing point is connected to the inverted Input pf the op-amp the circuit will produce the negative Sum of any number of Input Voltage likewise when the Summing Input is Connected to the non Inverting Input of the om-amplifier it will produce the Positive Sum of the Input voltages.