NAME Adnan Khan

Id 14837

Semester BS(CS) 4th

Subject Computer Architecture.

Assignment No 1.

Q1 What are main

Ans:- Data processing:-
Data may take a wide variety of forms & the range of processing requirments is broad.
Data storage:-
The computer perform a log term data storage function file of data is stored.
Data movements:-
When data is moved over longer distances, to or form is called data communication.
Control:-
Within the computer, a control unit manages the computers resources the performance of its functional parts in response to instructions.

Q2 Figure 01 shows the IBM Z Enterprise Ec 12 core layout briefly. Explain the function of each area.

Ans: ISU (Instruction Sequence Unit):-
Determines the sequences in which in which instruction are executed in what is reffered to superscalar architecture.
IFU (Instruction fetch Unit):-
logic for fetching instruction.

IDU (Instruction decode unit):-

Is responsible for parsing & decoding of all z/architecture operation codes.

LSU (load-store unit):-

it is responsible for handling all types of operand access of all lengths in the z/architecture.

XUC (translation unit):-

This unit translate logical addresses from instruction into physical adresses in the main memory. It contain TLB used to speed memory acess.

FXU (fixed point unit):-

The FXU executes fixed-point arithmetic operations.

BFU (binary floatin unit):-

The BFU handles all binary & hexa-decimal floating operations as well as fixed point multiplication operations.

DFU (decimal floating point unit):-

The DFU handles both fixed point & floating point operation on number that are stored as decimal digits.

RU (recovery unit):-

The RU keep a copy of the complete state of the system

Cop (dedicated co-processor):-

The cop is responsible for data compression

& encryption function for each core.

L1 cache:-

There is a 64-Kb L1 instruction code cache allowing the ifu to prefetch instruction before they are needed.

L2 control:-

This is the control logic that manages the traffic through the two L2 cache.

Data L2 :-

A - 1MB L2 data cache for all memory traffic through the two L2 cache.

Instr - L2:-

A1 - MB L2 instruction cache.

Q3 Discuss the IAS operation using the flowchart in fig Q2.

Ans:- The IAS operates by respectively performing as instruction cycle each instruction consist of two sub-cycle.

Fetch cycle:-

The op code of next instruction is loaded into the IIR & the address portion is loaded into the MAR. This instruction may be taken from the IBR, or it can be obtained from memory by loading a word into MBR, & then down to the IBR IR & MAR.

Executive cycle:-
The control circuitry interepts the the opcode & execute the instruction by sending out the appropriate control signals to cause data to be moved or an' operation to be performed by ALU.

D. For each of the following example, determine whether this is an embeded system explaining why or why not.

a. Are programs that understand physics &/or hardware embeded? e.g one that uses finite-element methods to predict fluid flow over airplane wings.

Ans) No, these programs are never considered to be embeded because they are not an integral component of a larger system.

b) Is the internal microprocessor controlling a disc drive an example of an embeded system.

Ans) Yes, regardless of what the disc drive is used for. The software (firmware actually) with in the disc drive control the HDA hardware & is hard real time as well.

c. I/O drives control hardware, so does the presence of an I/O driver simply that the computer executing the driver is embeded?

Ans No I/o drivers do not represent the embedded system.

d. Is the microprocessor controlling the cell phone an embeded system?

Ans Yes the firmware in the cell phone is controlling the radio hardware.

e. Are the computer in a big phased array radar considered embeded? These radios are 10 story buildings withe one to three 100-foot diameter radiating perches on the stoped slides of the buildings.

Ans Yes these computers were generally some of the most powerfull computers available when the system was build, are located in large computer room occupying almost one whole floor of a building & may be hunderds of meter away from the radar hardware. However the software running in these computer control the radar hardware therefore the computer an integral component of a large system.

f. Is a PDA an embeded system?

Ans Yes, PDA is an embeded system because its just like a personal computer in hand.

g. Is a traditional flight mangement system (fms) buit into an airplane cockpit considered embeded?

Ans If the FMs is not connected to the avoinics & is used only for logistice computerization, a function readily performed on a laptop. then the FMs is clearly not embeded.

h. Are the computer in a a hardware in the loop (HIL) simulator embeded?

Ans Yes, both in the simulator & in the thing being tested in the HIL simulator hardware is being controlled on both side.

i. Is the computer controlling fuel injection in an automobile engine embeded?

Ans Yes, its a part of a large system, the engine & its directly monitoring & controlling the engine through special hardware.

j) Is the computer controlling a pacemaker in a person's chest an embeded computer

Ans Yes in this case of the system is the

combination of the pacemaker & the person's heart.

Q Write note on the following.

/

A:- Main structural components of a computer.-

There are four components of main structural:-

* CPU:-

Control the operation of the computer & performs it data processing functions, often simply refered to as processor.

* Main memory:-

Stores data.

* I/O:-

Moves the data between the computer & its the external movements.

* System interconnections:-

Some mechanism that provides for communication among CPU, main memory & I/O.

b. Key characteristice of a planned computer family.

Ans Similar or identical instruction sets:-

In some cases the lower end of the family has an instruction set that

Date: / /

is a subset of that of the top end of the family. This mean that program can move up but not down.

* Similar or identical operating system:-
The same basic operating system is available for all family members.
* Increasing speed:-
The rate of instruction execution increases in going from lowe to higher family members.
* Increasing numbers I/o parts:-
The number of I/o parts increases in going from lowe to higher family members.
* Increasing memory size:-
The size of main memory increases in going from lower to higher family members.
* Increasing cost:-
At a given point in a time the cost of a system increases in going from lower to higher family members.

c) Stured program counter.

Ans A fundamental design uproach first implemented in the IAS computer is known as stored program counter. This idea is usuall attributed to the mathematician

* The first publication of the idea was in 1945 proposal by von neuman for a new computer the EDVAC.

In 1946, Von neumaan & his collagues began the design of a new stored program computer, referred to as the IAS computer, It consists of.

* Main memory which stores both data & instructions.
* An arithmetic & logic unit (ALU) capable of operating on binary data.

D) Moore's Laws-

Moore's Law was prefound by gordon moore cofounder of intel in 1965 (Moor65). Moore observed that the number of transistor that could be on a single chip was doubling every year.

The consequence of moore's law are pretaund.

1) The cost of computer logic & memory circuitry has fallen at a dramatic rate.
2) Becavse logic & memory elements are placed closer together on more densely pack chips, the electric path length is shortened increasing operating speed.

3 There is a reduction in power requirements.

4 With more circuitary on each chip there are fewer interchip connections.

Differentiate each of the following.

A) Computer organization & computer architecture.

Ans Computer organization:-

refers to those attributes of a system visible to a programmer or put another way those attributes that have a direct impact on the logical execution of a program. A term that is often used interchangbly with computer architecture is instruction set architecture.

Computer architectures-

refers to the operational unit & their interconnection that realize the architectural specification example of architectural attributes include the instruction set the number of bills used to represent various data types (e.g numbers, characters) I/O mechanism & techniques for addressing memory.

B) Microprocessor & Microcontrollers:-

Ans Microprocessors:-

Chips include registers an ALU & some sort of control unit or instruction processing logic. A transistors density increased it became possible to increased it ultimately to add memory & more than one processor.

Microcontroller:-

is a single chip that if contains the processor, non-volatile memory for the program (Rom) volatile memory for input & output (RAM) a clock & an I/O control unit. The processor portion of the microcontroller has a much lower silicon area than other microprocessor & much higher energy efficiency.

c) Risc and Cisc:-

The current X86 offerings represent the result of decades of design effort on complex instruction set computers (CISC). The x86 incorporates the sophisticated & serves as an excellent example of CISC design. An alternatives approach to processor design is reduced instruction set computer (RISC). The ARM achitecture is used in a wide variety of embeded system &

Date: / /

is one of the most powerful & best designed Risc based system on the market in this section & the next we provide a brief overview of these two system.

D) Cortex - A, Corten - B & Corten - M

The corten A & Corten - A50 are application processor intended for mobile devices such as smartphones & eBook readers, as well as consumer devices such as digital tv & home gateways (e.g DsL & capable internet modems). These processor run at higher clock freqvency (over 1 GHz) & support a memory managment unit (MMV).

* The corten - R is designed to support real time applications, in which the timing of events need to be controlled with rapid response to events. They can run at a fairly high clock frequency & have very low response latency.

* Corten - M series processor have been developed primarly for the microcontroller domain where the need for fast, highly deterministic interput mangement is coupled with the desire fore extremely low gate coont & lowest possible power consumption.

Q4 Solve each of the following.

A Given the memory contents of the IAS computer show below,

Address contents.

1. 08A010FA2/0FB
2. 08B010FA0F08D
3. 08c020FA2/0FB

A Show the assembly language code for the program, starting at adress 08A.

Ans Here is a simply way to understand this problem contents are divided upt into two 5 bit instruction LH & RH.

LH instruction = 010FA

Opcode = 01

address = 0FA

RH instruction = 210FB

Opcode = 21

adress = 0FB

Since in this Hexadecimal form you have to convert the number to binary form (use the IAS instruction set)

LH instruction:-

01 = 00000001 = Load M(x)

M(x) refer to the memory address location 0FA The first 5 Bits of 08A should read - load M(0FA) RH instruction.

21 = 00100001 = Stor M(x)

Date: / /

M(x) refer to the memory address location OFB

The second 5Bits of 08A should read stor M(OFB)

Finally the assembly language code for 08A 010FA210FB is

LOAD M(OFA)

STOR M(OFB)

2. Here is a simply way to understand this problem.

contents are divided up into two 5 Bits instruction LH & RH

LH instruction = 010FA

Opcode = 01

address = OFA

RH instruction = 0F08D

Opcode = 0F

address = 0BD

Since this is in heradecimal form you have to convert the number to binary form.

LH instruction:-

01 = 00000001 = Load M(x)

M(x) refers to the memory address location 08D.

The first 5 Bits of 08B should read- jump + M(08D, 0:19)

Finally the assembly language for 08B 010FA0F08D is Load M(OFA)

jump + M(08D, 0:19)

3. Here is a simple away to understand this problem contents are divided up into 5 bits instruction LH & RH

LH instruction = 020FA

opcode = 02

address = 0FA

RH instruction = 210FB

opcode = 21

address = 0FB

Since this in hexadecimal from you have to convert the numbers to binary form.

LH instruction.

02 = 00000010 = Load - M(x)

M(x) refere to the memory address location 0FA

The first 5 Bits of 08C Should read- load - M(0FA)

RH instruction

21 = 00100001 = STOR M(x)

M(x) refers to the memory address location 0FB.

The second 5 Bits of 08C Should read - stor M(0FB)

Finally the assembly langvage code for 08C 020FA210FB is

Load - M(0FA)

STOR M(0FB)