

Department of Electrical Engineering
Assignment

Date: 20/04/2020

Course Details

Course Title: _____

V.L.S.I

Module: _____

Instructor: _____

Engr. Zulqarnain

Total Marks: _____

Student Details

Name: _____

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Student ID: _____

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Part A (Objective Type)

1. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance??
 - a. Static dissipation
 - b. Dynamic dissipation
 - c. Both a and b
 - d. None of the above.
2. Which type of MOSFETS Exhibits no current at zero gate voltage?
 - a. Depletion MOSFET
 - b. Enhancement MOSFET
 - c. Both a and b
 - d. None of the above
3. CMOS circuits are constructed in such a way that all PMOS transistors must have either an input from the voltage source or from another
 - a. PMOS transistor
 - b. NMOS transistor
 - c. CMOS transistor
 - d. BJT transistor
4. Delay which is equal to the time taken by a gate output transition to 0, from another value 1, x, or z is
 - a. Rise delay
 - b. Fall delay
 - c. Turn-off delay
 - d. Turn-on delay
5. Which type of simulation model is used to check the timing performance of a design?
 - a. Transistor level
 - b. Gate level

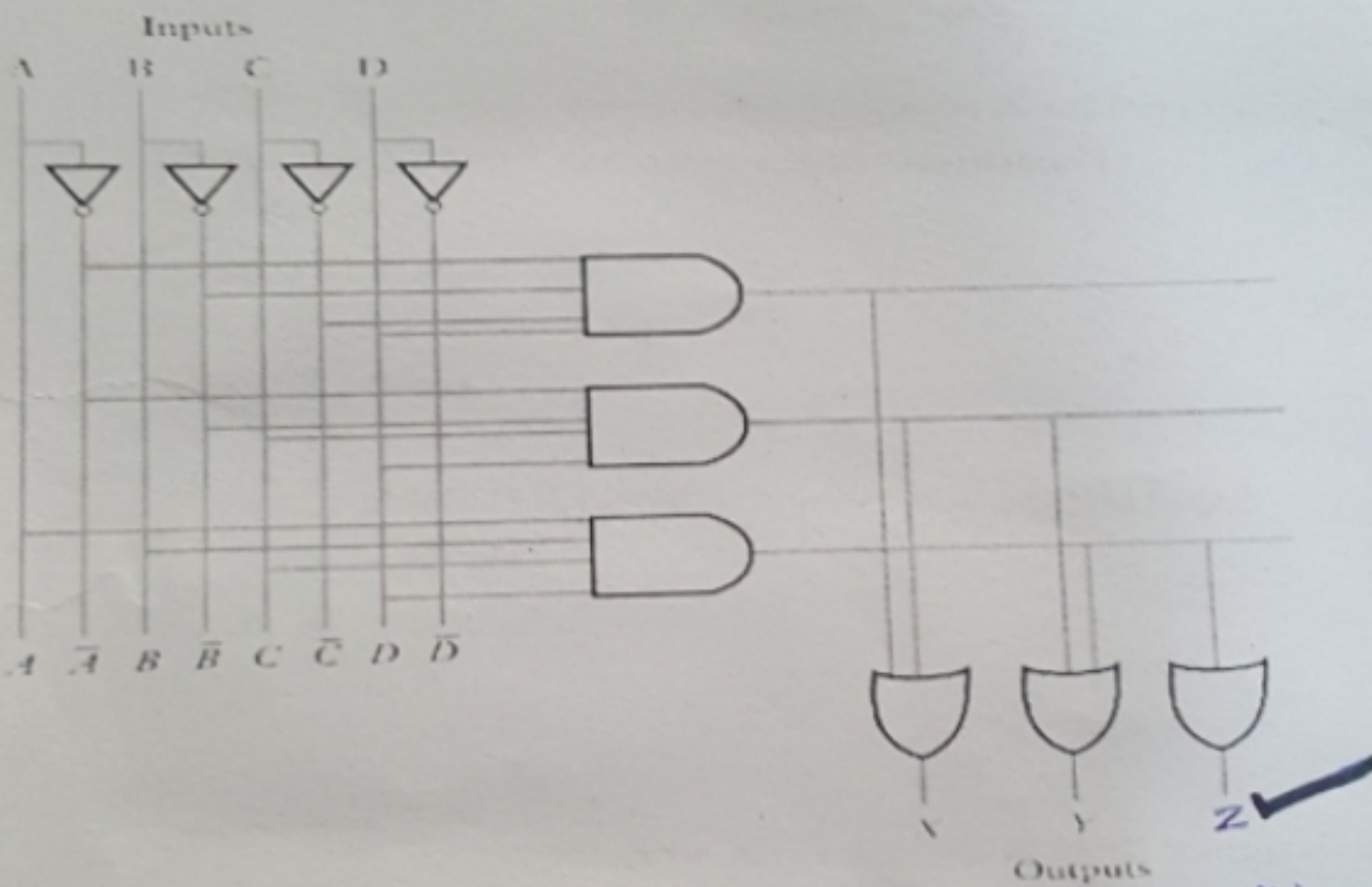
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- c. Behavioral
- d. Switch level
- e. None of these

6. Which of the following statements is incorrect
- a. Some PLDs are programmed using electrically operated switches.
 - b. Some PLDs are programmed using mechanical switches

Fill in the Blanks

7. In MOS devices, the current at any instant of time is Constant & independent of the voltage across their terminals.
8. For complex gate design in CMOS, OR function needs to be implemented by connections of MOS \rightarrow Parallel
9. In the following PLA, which output implements the logic function ABCD??



10. The term VLSI means a device containing between Thousand and Million transistors.

Part B (Subjective Type)

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Q1.		In low power VLSI design clock gating technique will reduce power all time or it depends upon the input data? Is any chance, the computation power may increase? (5)
Q2.	(a)	If we want to design an IC and I want that each and every transistor used in this IC should be optimized individually with less time. How it will be possible?? (5)
	(b)	While fabrication of NMOS or PMOS we usually use inorganic polymer. If we use organic polymer instead of inorganic polymer what will happen?? (5)
Q3.		Draw a stick diagram of a layout using that variable ordering $F = \overline{ACD} + \overline{ABD}$ (5)

Q01
(101)
AnsClock Equating Technique:

The clock equating technique using the flip-flop clock only when the output has to change. clearly its mean that flow will clock less the circuit that in the previous one.

* In reality when this is done via the synthesis tool rather than just one and a latch integrated cell in the library used and the present latch is used with the end timing of the clock and enable are different clock-tree synthesis. these are main may also be added observability to different reason. clearly a equating structure would not be applied to every register. The cost power in the equating would exceed saving on a flop.

Q (A)
 (Ans)
 Q (A)

A Transistor is a semiconductor device used to amplify or switch electronic signals and electrical power. It is composed of semiconductor material usually with at least three terminals for connection to an external circuit.

A voltage of circuit applied to one external circuit. A voltage of circuit applied to one pair of the transistor terminal controls the current through another pair of terminal. B-C the control (out-put) power can be ~~very~~ higher than the controlling (input) power a transistor can amplify.

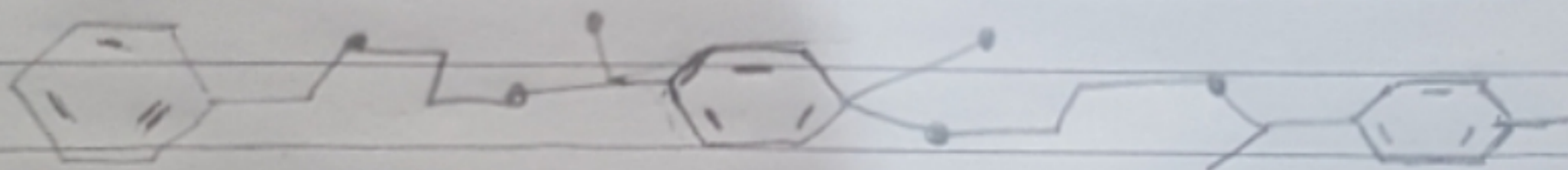
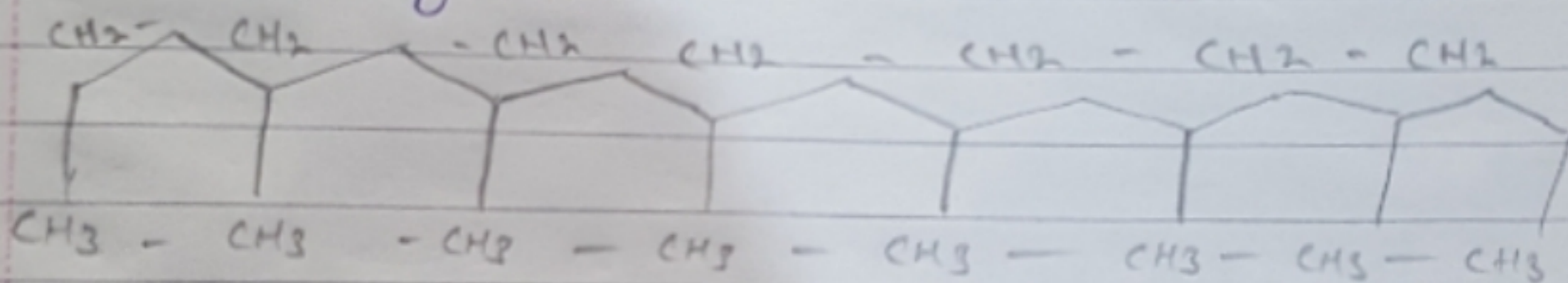
* Today some transistor are packed individually but many more are found embedded in integrated circuit.

* The more transistor are in circuit faster and data processed.

Q.02
Ans (B)Organic Polymers

Organic polymers are polymeric material that essentially contain carbon atoms in the back bone. therefore these are only carbon covalent bond in

* These polymer only form organic monomeric molecules. most of the times, these polymers are environmental friendly since are bio degradable.



* Further more these are two major forms of organic polymers such as natural and synthetic polymers. Common Example of important organic polymers.

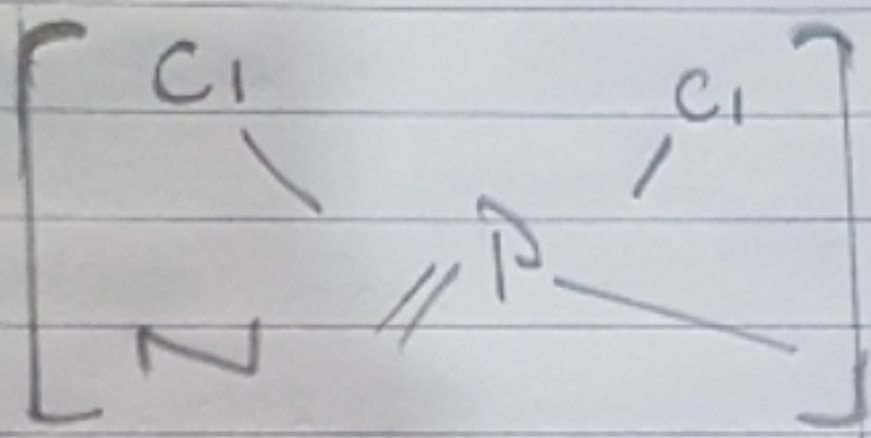
(Polyamide, proteins, polynucleotides, (DNA & RNA) etc.

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Inorganic polymers Material that have no carbon atoms in the back-bone. However most of these are some organic regions as well. Materials are highly branched structures and have chemical elements other than carbon.



These polymers are not environmentally friendly. B.C they are not biodegradable.

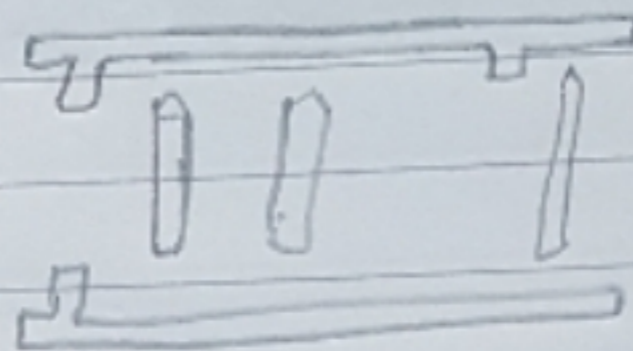
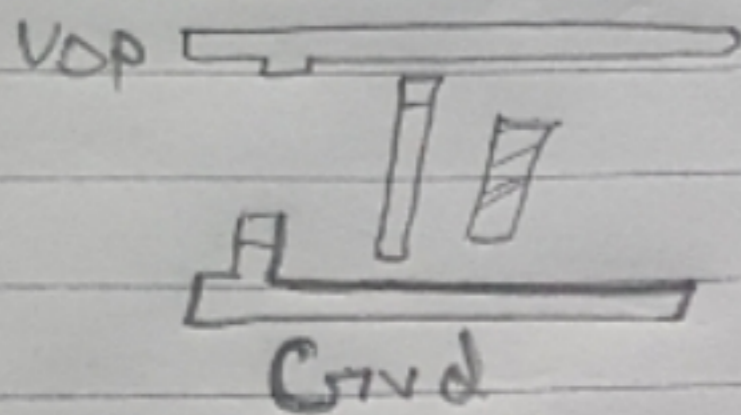
C.x. include polydimethylsiloxane is

(Silicon, rubber, polyphosphazenes etc.)

Ans⁽⁰³⁾ Stick Diagram.

Stick Diagram help plan input quickly.

- Need not be to scale.
- Draw with colour pencil or dry erase markers.



* Wiring Tracks:

A wiring track is the speed required for a wire $4n$ with $4x$ spacing from neighbor = 8Δ pitch.

- Transistor also consume one vstoy track.

* Well Spacing.

We must surround transistor by $6n$ implies $1n$ $6n$ opposite transistor flows.

- Leaves room for one wire track.

* Area Estimation - Estimation area by counting wires track.
- Multiple by 8 to express in μ