Digital Logic Design:

Assignment: 8.

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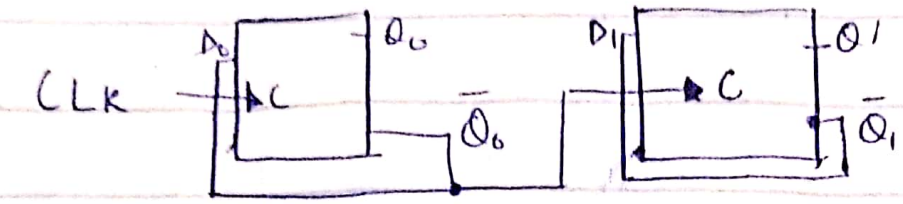
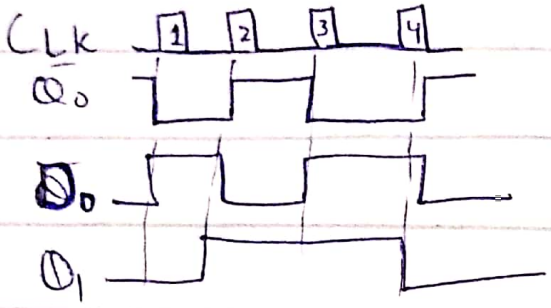
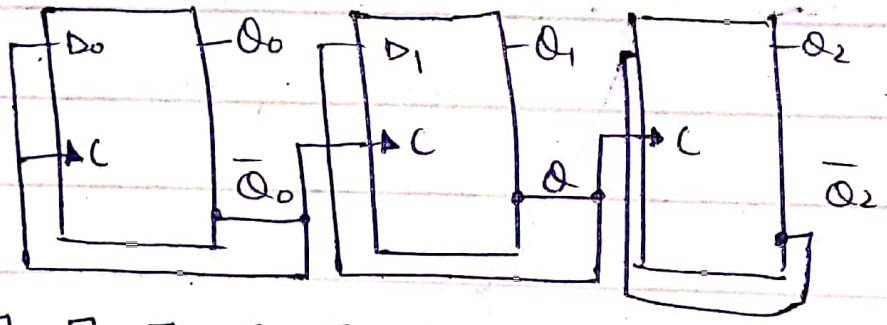
Q. 1

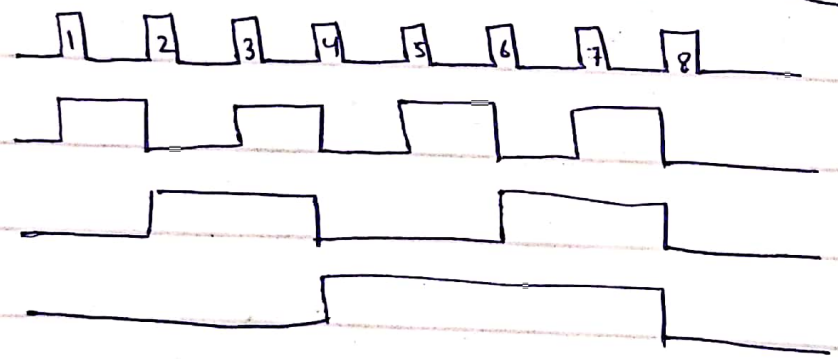




Clock pulse	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (Recycle	0	0

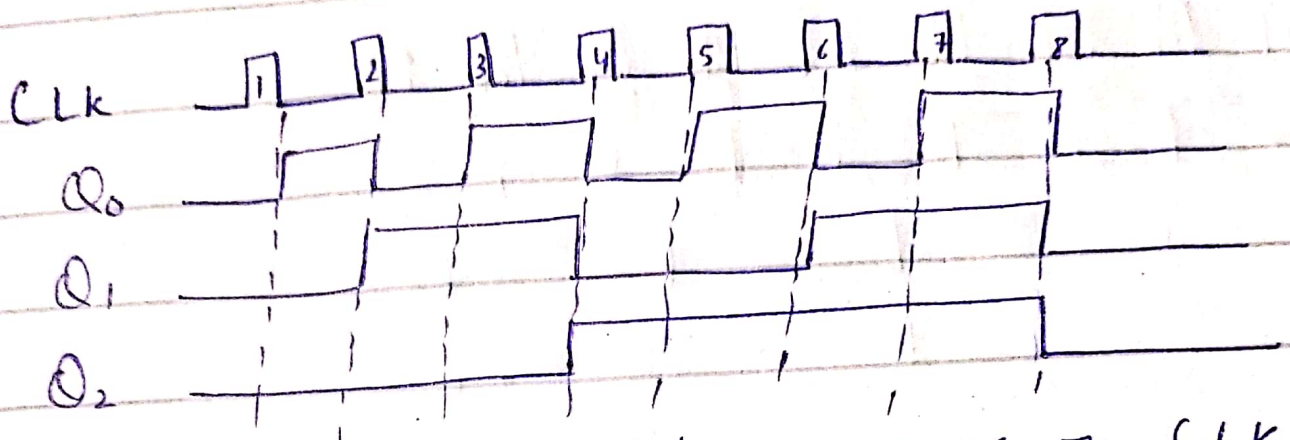
Q:2)





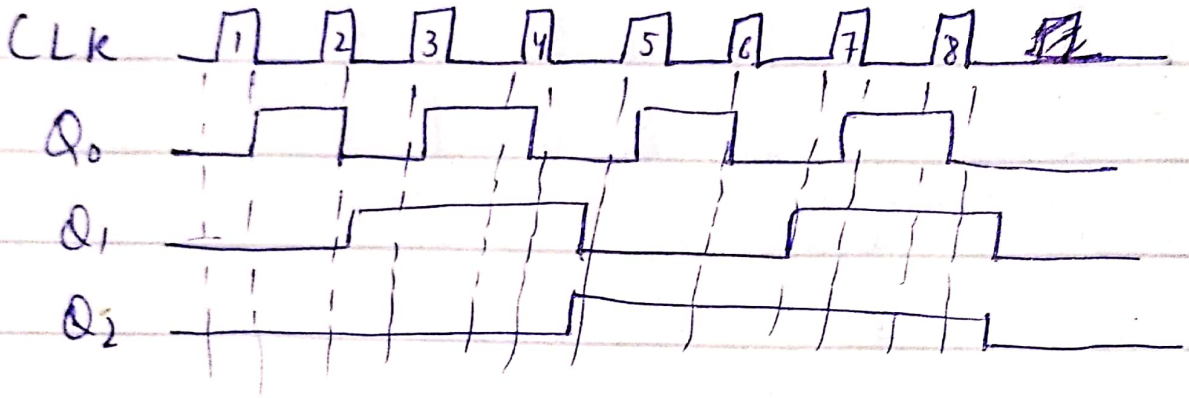
C. Pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8 (Recycle	1	1	1

Q: 3)



The worst case delay occurs on CLK - Q_0, The high delay is 8ns, because in the case of sychoronous binary, the propogation delay is independant of the number of flip-flop used.

Q: 4)



The worst case delay occurs at Q_2

The delay interval equals to three times the delay time at Q_2.

$$3(8ns) = 24ns.$$