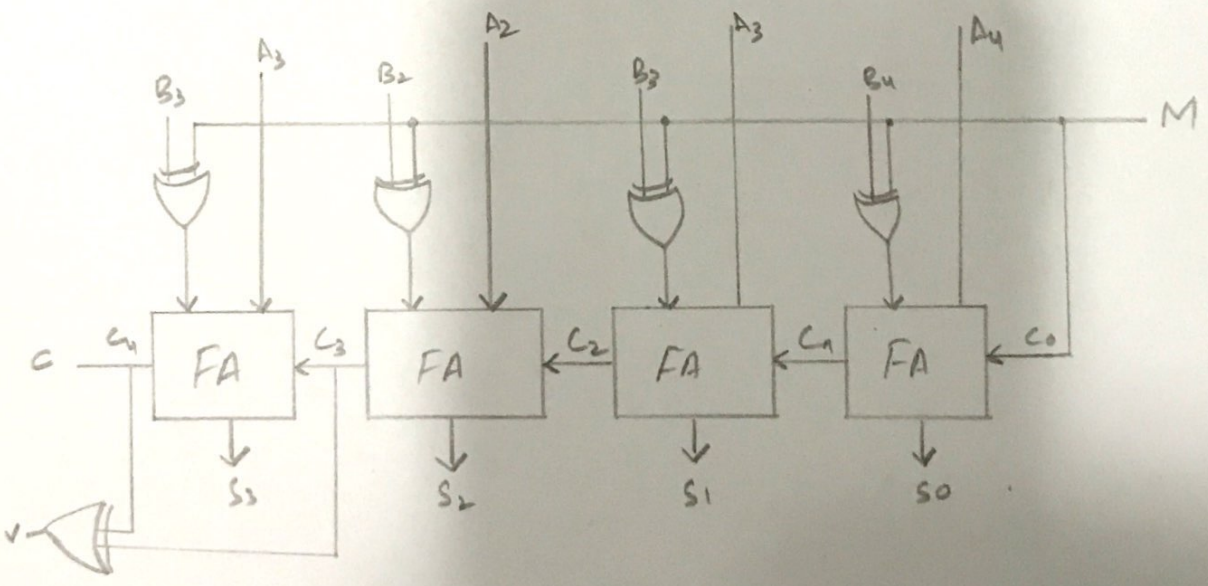
Q1 Draw & explain the logic diagram for each of the following.

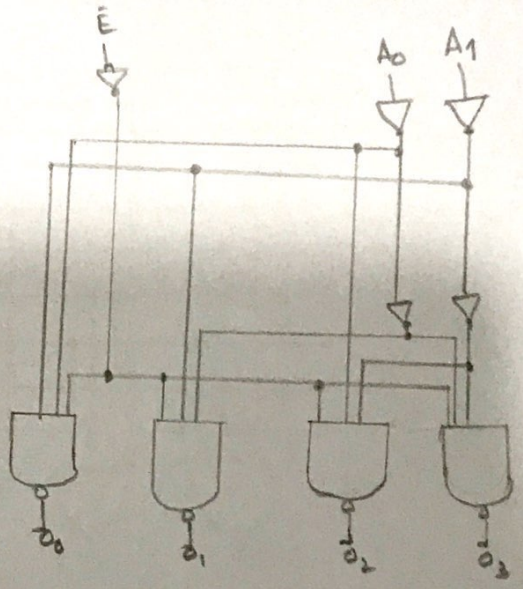
a/- Four-Bit Adder-Subtractor

The addition & subtraction operation can be combine into one circuit with one common binary adder by including an exclusive-OR gate with each full adder. A four-bit adder-subtractor circuit is given below.



Q1

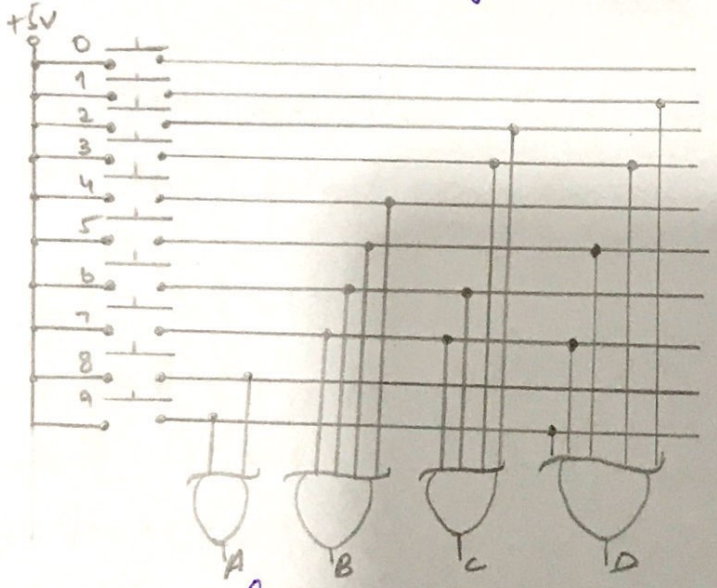
b|- Notice how NAND gates are used instead of ANDs as i have used in part a. Thats why decoder output are typically active low. Recall that NAND gates are the simplest gates to make, requiring fewer transistors & less space.



Q1

C1- Decimal to BCD Encoder.

Encoders are the electronic equipment which converts one form of input into another one. Encoders are used to generate a coded output from a single active numeric input.



In Decimal to BCD encoder binary output in the form of '1's & '0's which is calculated in encoder as below.

Equations:

A = 8+9

B = 4+5+6+7.

C = 3+4+6+7.

D = 1+3+5+7+9.

Q2 for the 4-input multiplexer, data inputs are given as.

Answer.

In multiplexer, the output Y takes the value of the input corresponding to the select bits. Select bits are S1S0.

Using this we can find the value of Y given the select inputs.

a) S0 = 1, S1 = 0

S1S0 = 01 (1 in decimal)

Thus, Y = D1 = 1.

b) S0 = 0, S1 = 1.

S1S0 = 10 (2 in decimal)

Thus, Y = D2 = 0.

c) S0 = 1, S1 = 1.

S1S0 = 11 (3 in decimal).

Thus, Y = D3 = 1.

d) S0 = 0, S1 = 0.

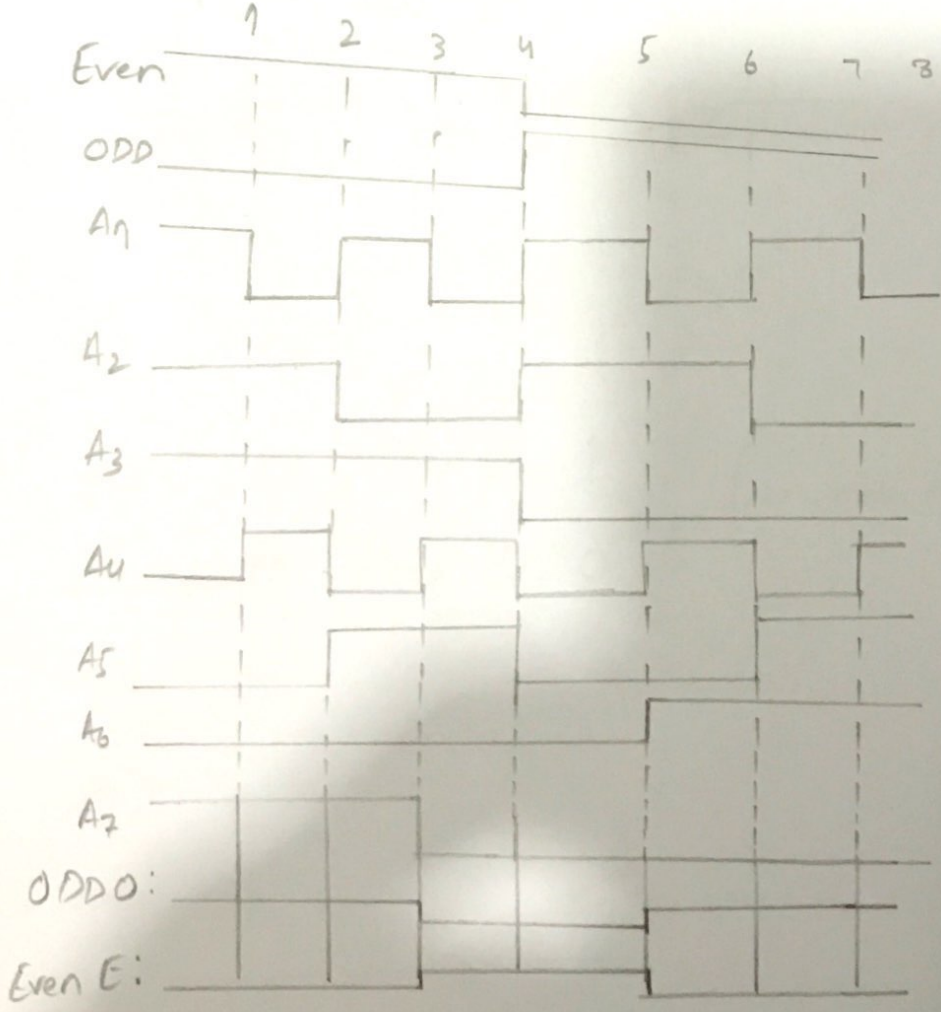
S1S0 = 00 (0 in decimal)

Thus, Y = D0 = 0.

Q3 Timing diagram in Figure Q1 shows inputs to a 9-bit parity checker. Draw the & Even & Σ odd output for the even parity checking.

Answer

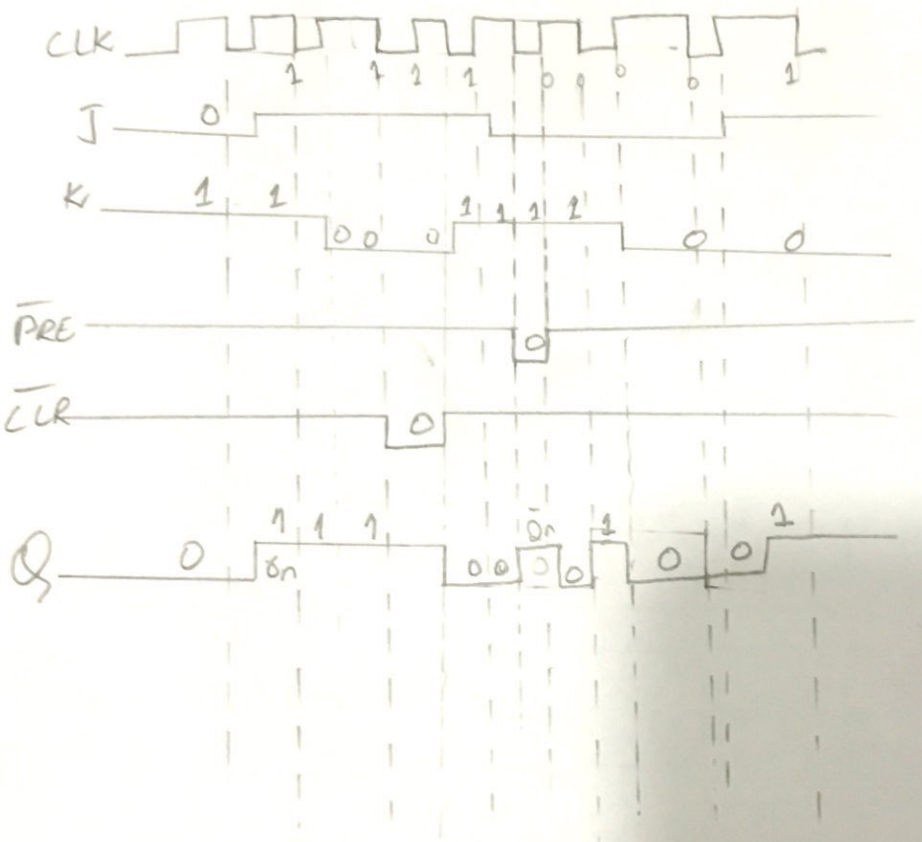
For 9 bit parity checker circuit, output is "1" when there are odd numbers of 1's in 9 bits otherwise output is "0". we will plot waveform based on above criteria.



From plot, we get
its even for bit time 1,2,3,6,7,8 &
odd for 4,5,6
Even = 6
odd = 3.

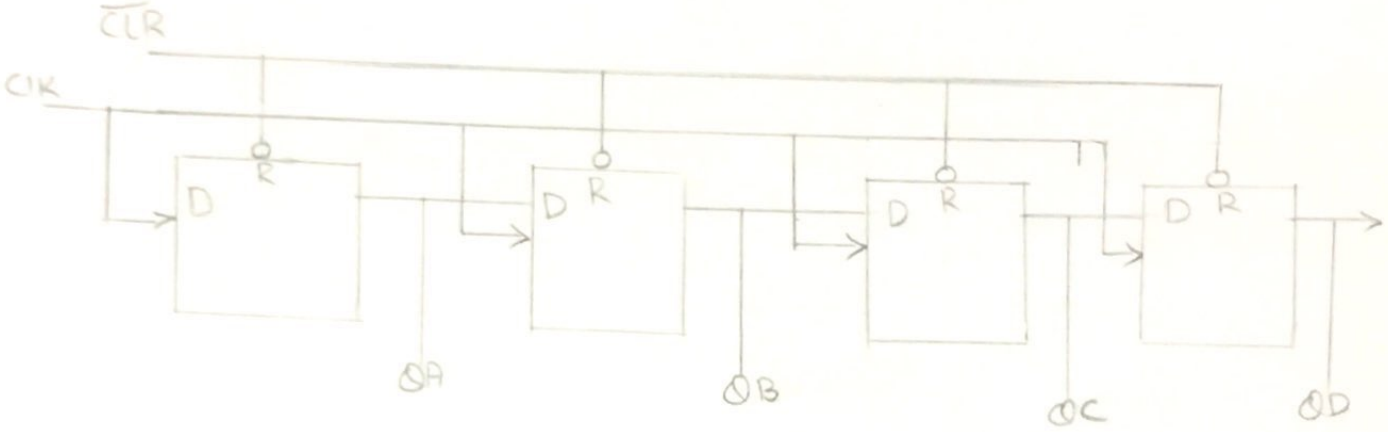
Q4 The wave in the figure 02 are applied to the J, K, CLK, $\overline{PRE}$ & $\overline{CLR}$ inputs as indicated. Determine the Q output, if the flip-flop is initially REST.

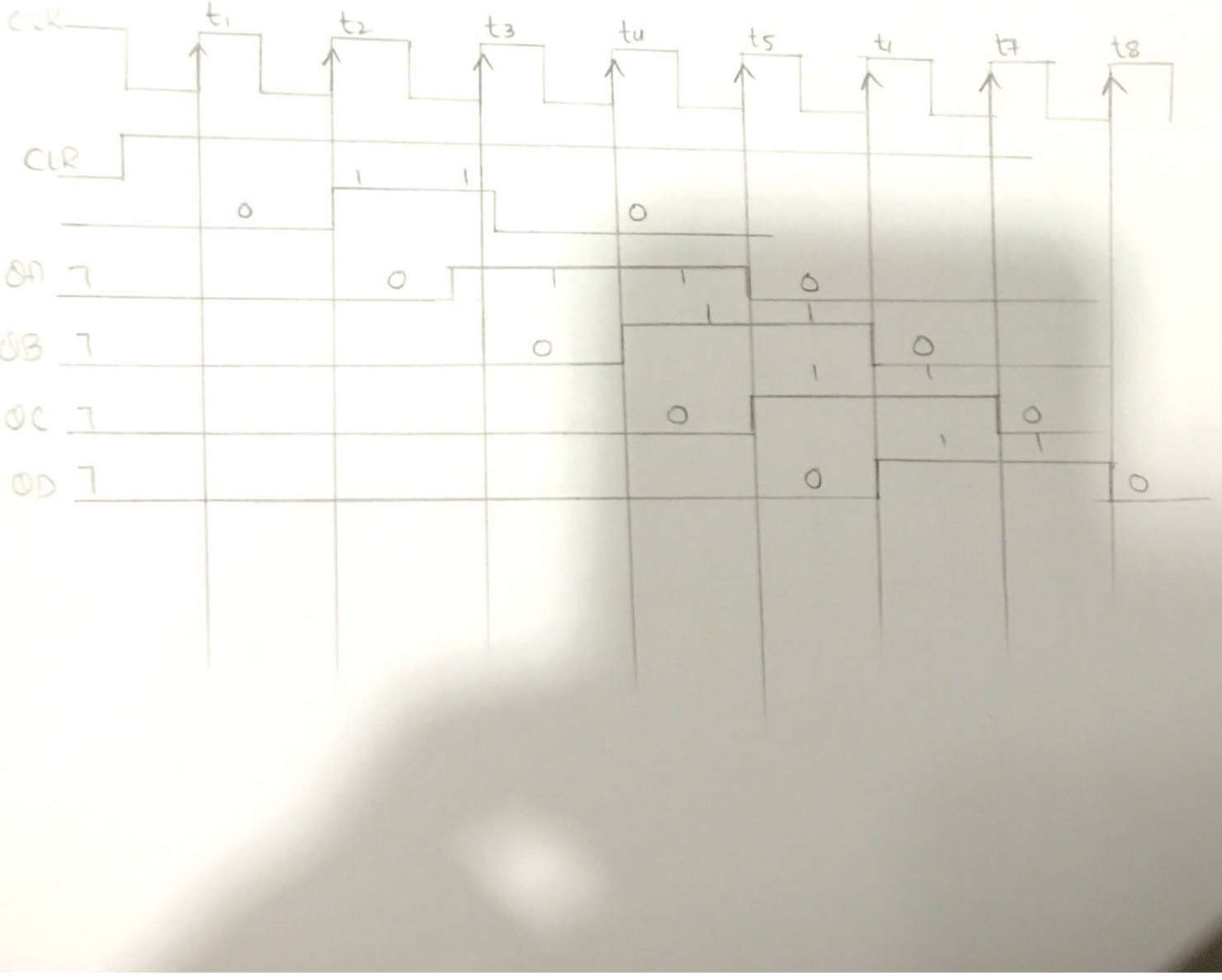
Answer.



$\overline{PRE} = 0$ O/P Q = 1
$\overline{CLR} = 0$ O/P Q = 0
} for one clock pulse.

Q5 Use the waveforms in figure 03 to draw the timing diagram for the parallel outputs (Q_1, Q_2, Q_3, Q_4) for the shift register. Assume that register is initially cleared.





Q6 Draw the logic diagram & timing diagram for the 4-stage synchronous binary counter. Verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.