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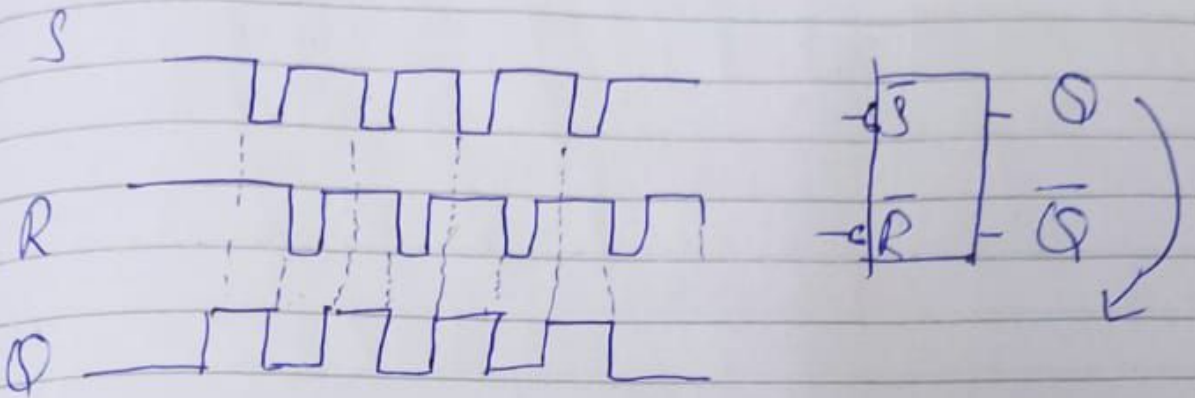
SUBJECT: DIGITAL LOGIC DESIGN

SEMESTER: 3<sup>RD</sup>

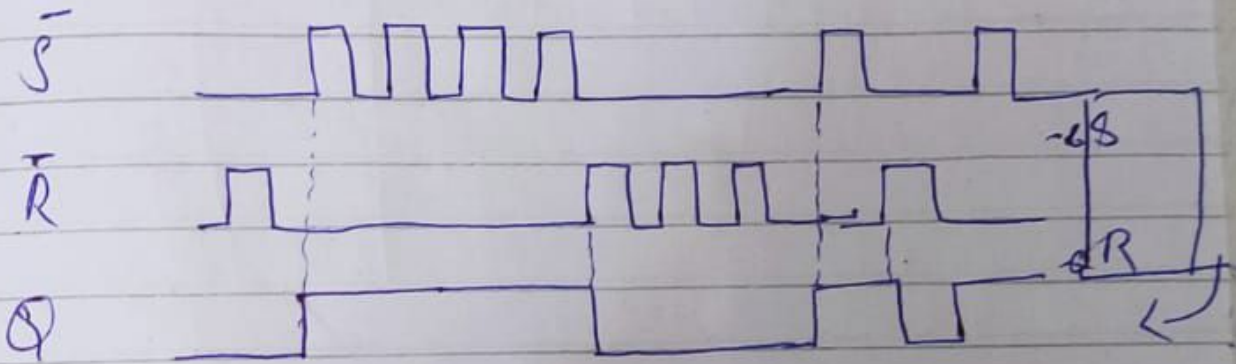
**PROGRAMME:** BS (SOFTWARE ENGINEERING)

①

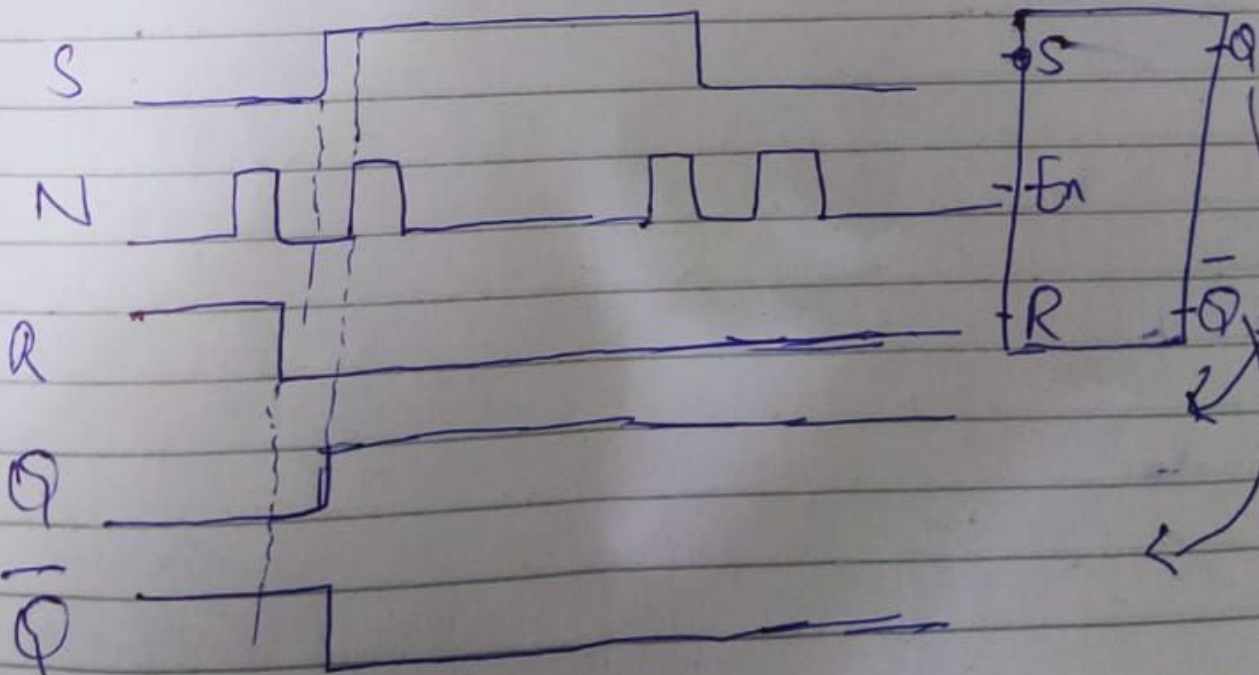
Q1)



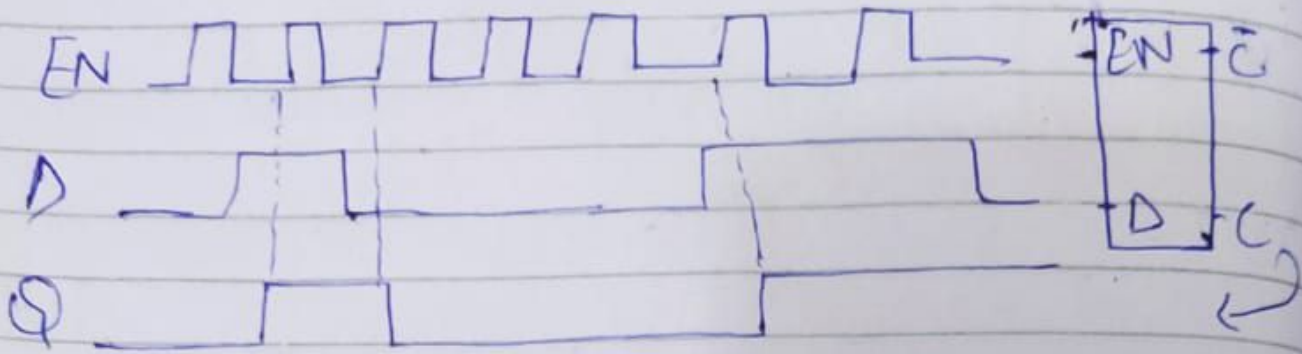
Q2



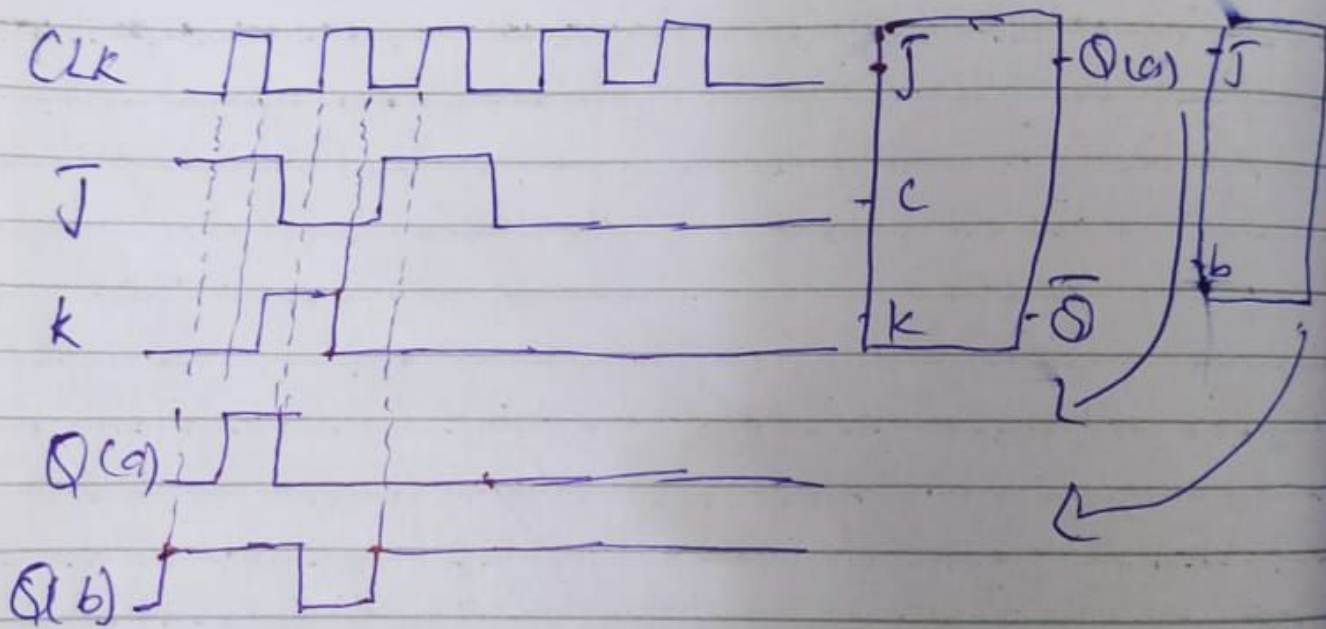
Q3



Q4



Q5



The main difference between (a) and (b) edge triggered JK-flip is that

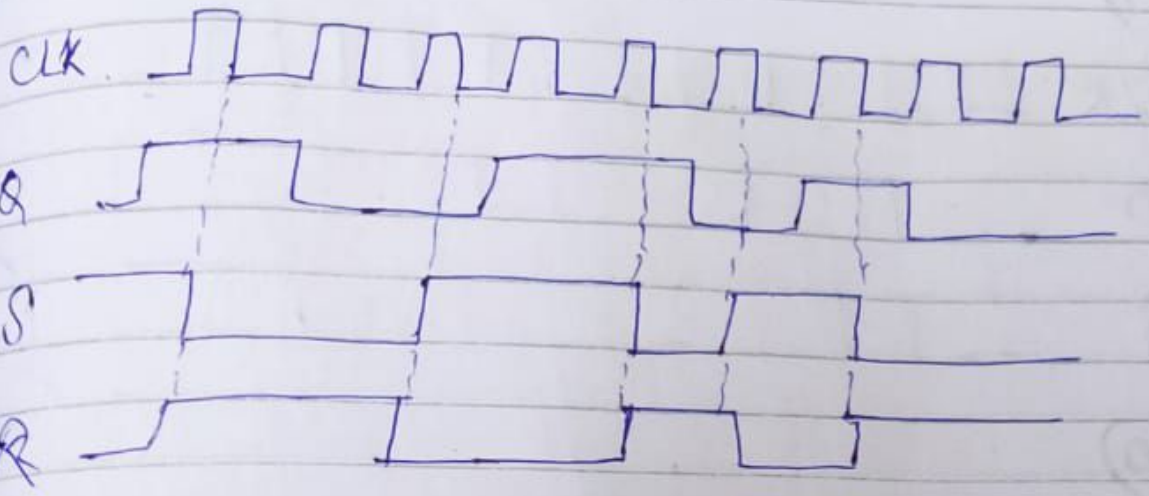
The flip flop (a) or the Negative edge and no clock pulse while

The flip flop (b) triggers on the positive edge of the clock pulse.

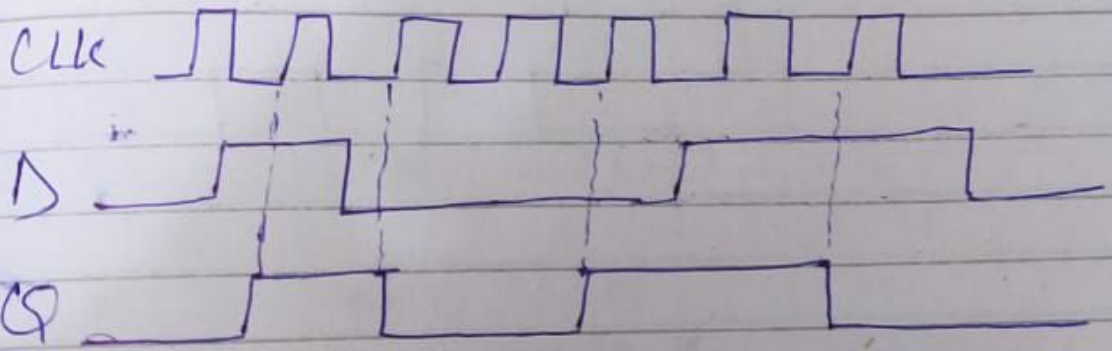


(3)

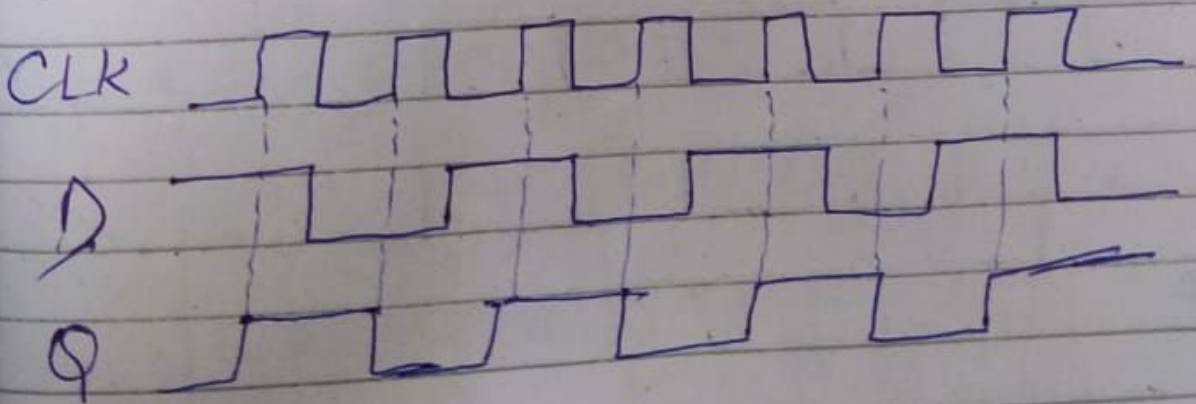
Q6



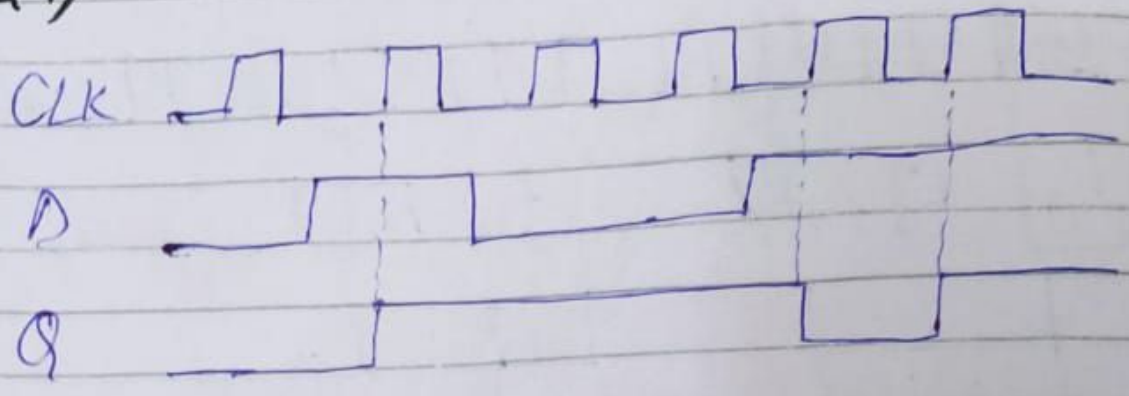
Q7



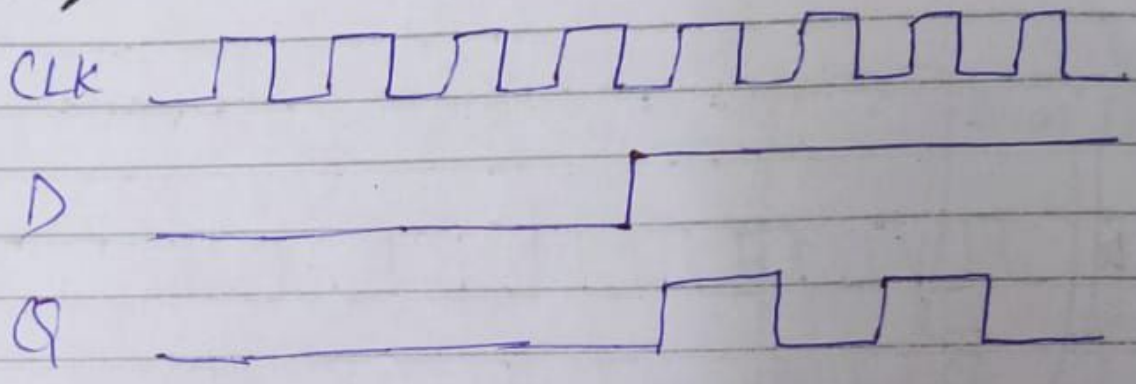
Q8



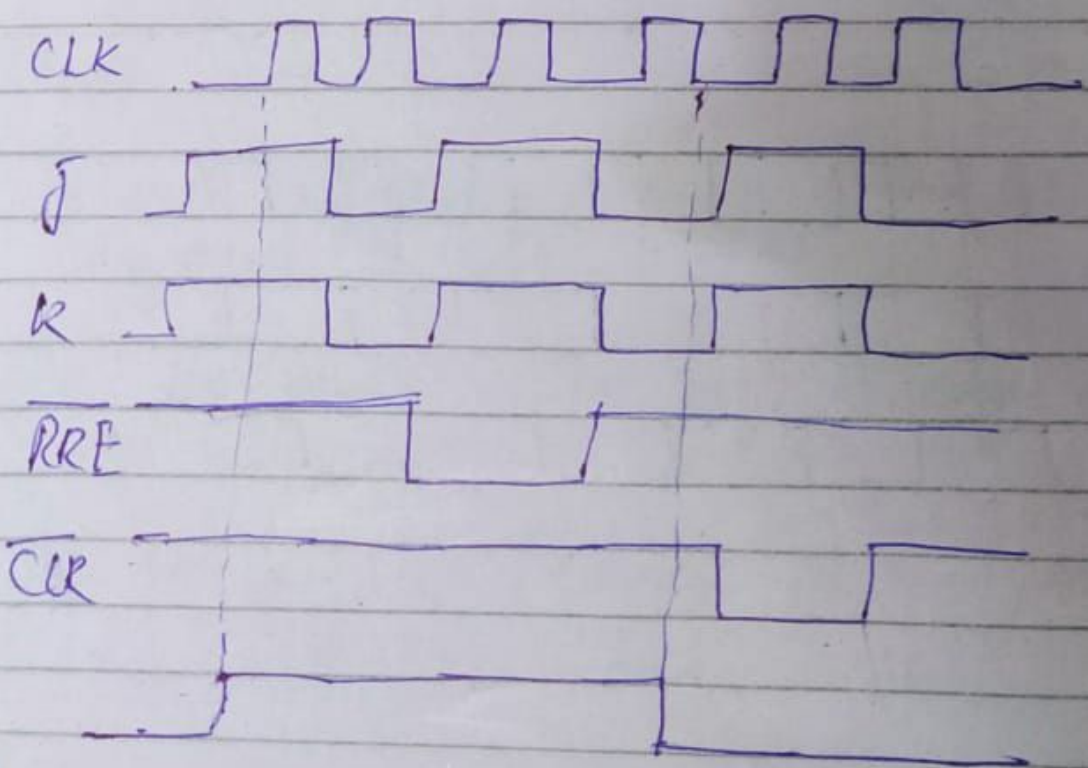
Q9)



Q10)

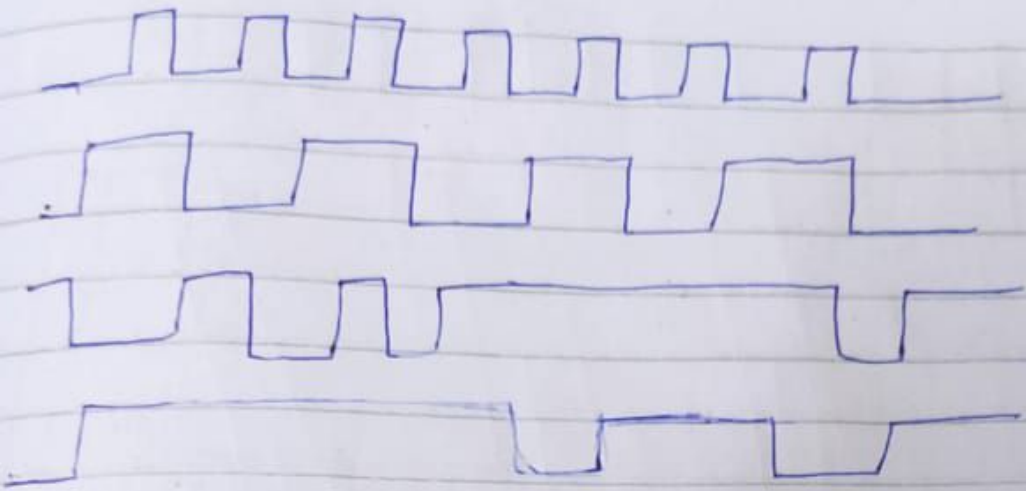


Q11)



(5)

Q12)



Q13)

$J_1 = 1010011$   
 $J_2 = 0111010$   
 $J_3 = 1111000$

$J_2 = 0010000$

$K_1 = 0001110$

$K_2 = 1101100$

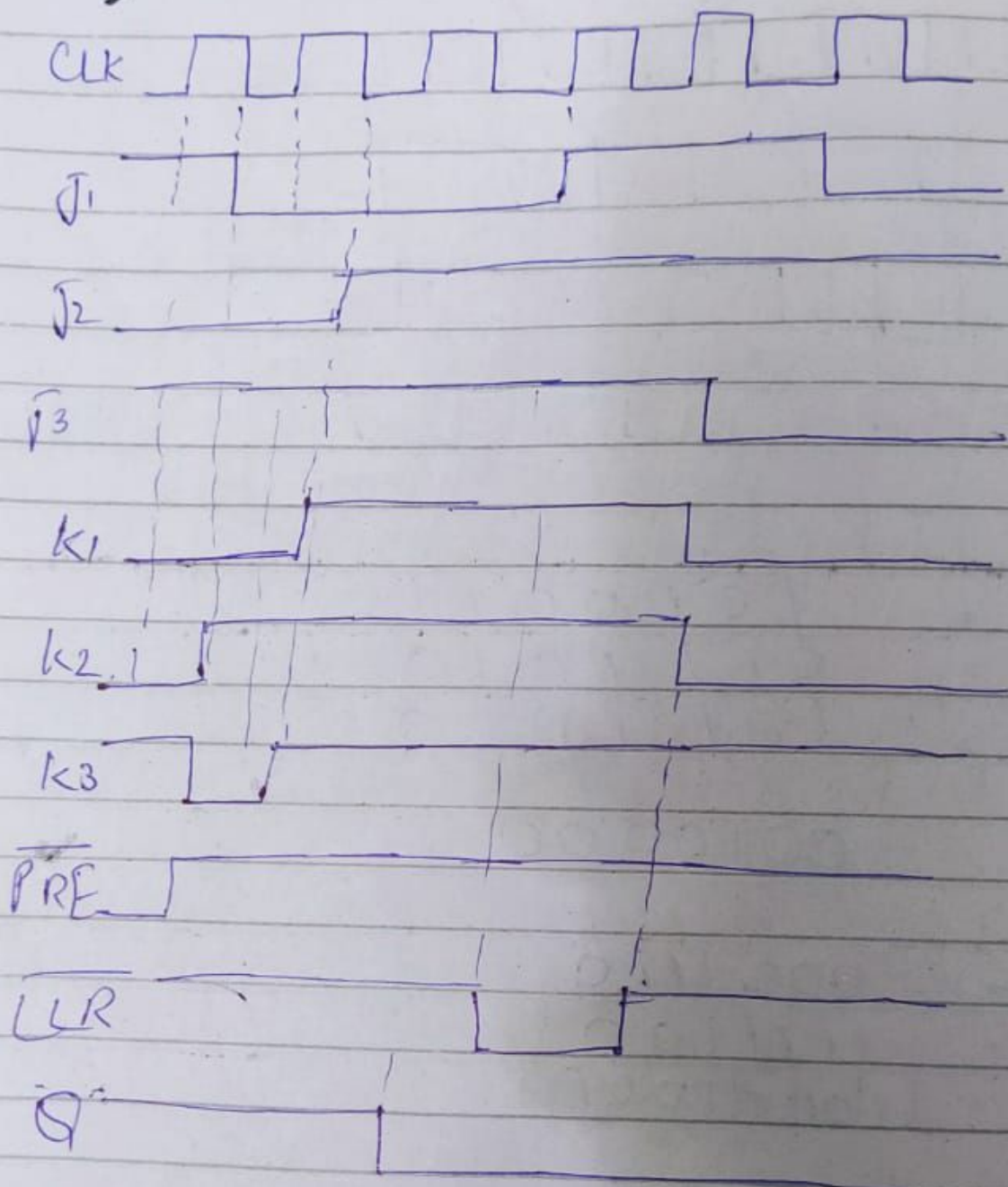
$K_3 = 10101001$

$K_2 = 0000100$

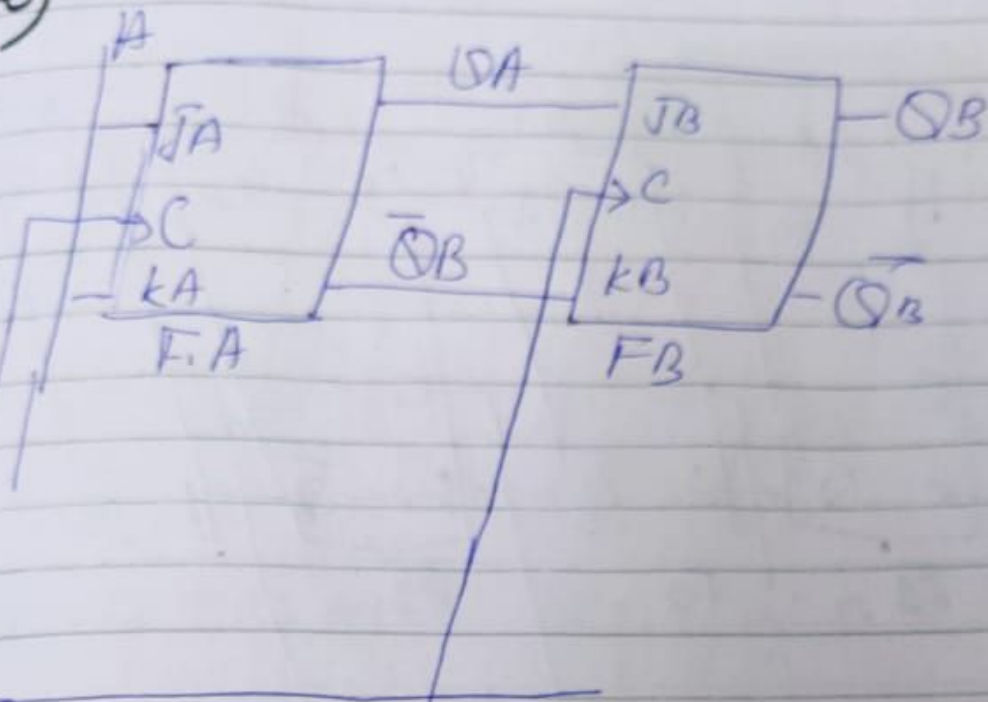
$J_2$	0	0	1	0	0	0	0
$K_2$	0	0	0	0	1	0	0
$Q_2$	0	0	1	1	0	0	0



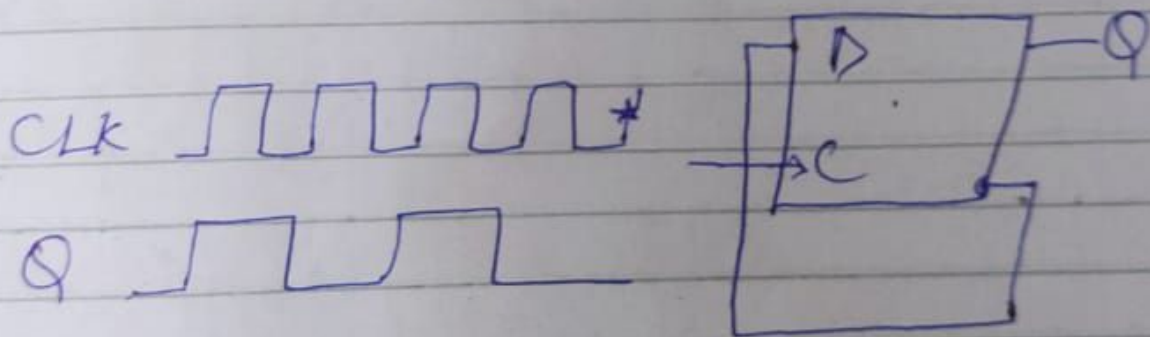
Q15)



Q16)



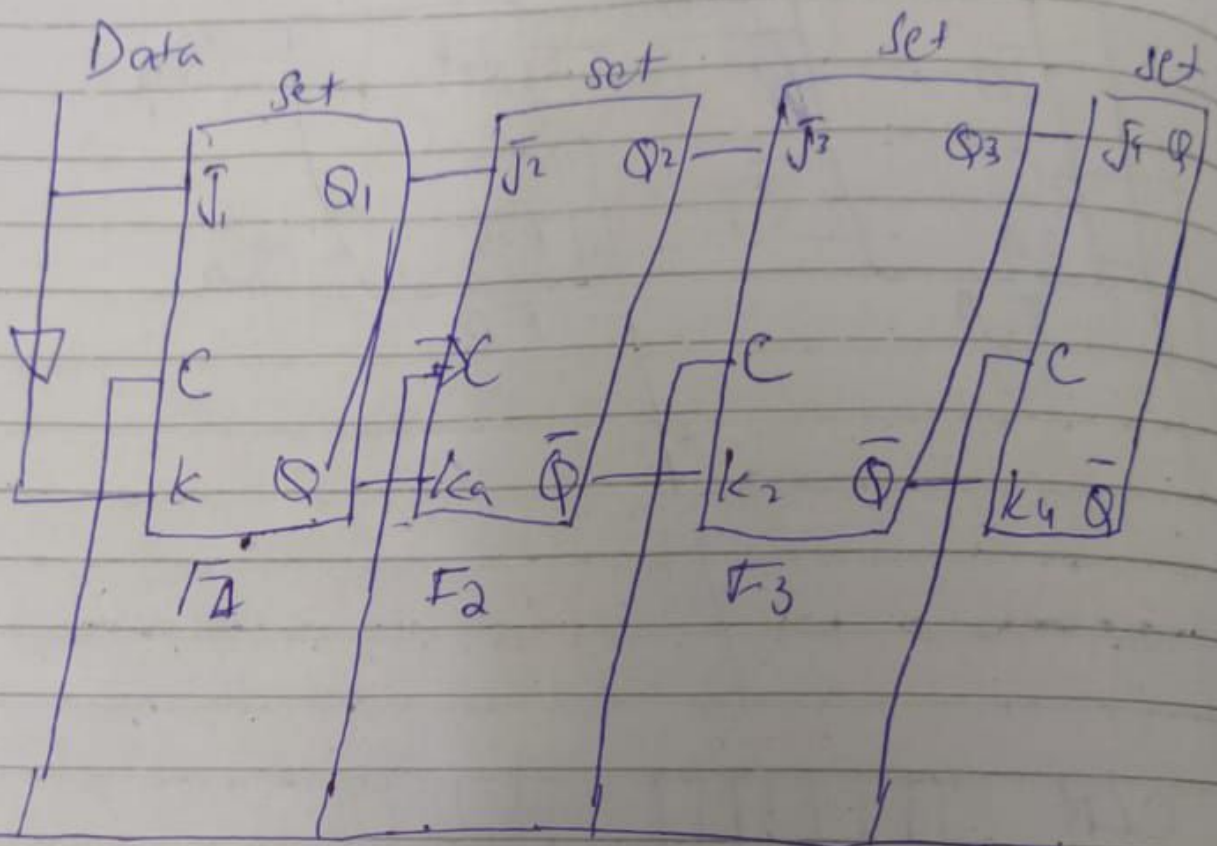
Q17



The device performs the Divide-by-two function



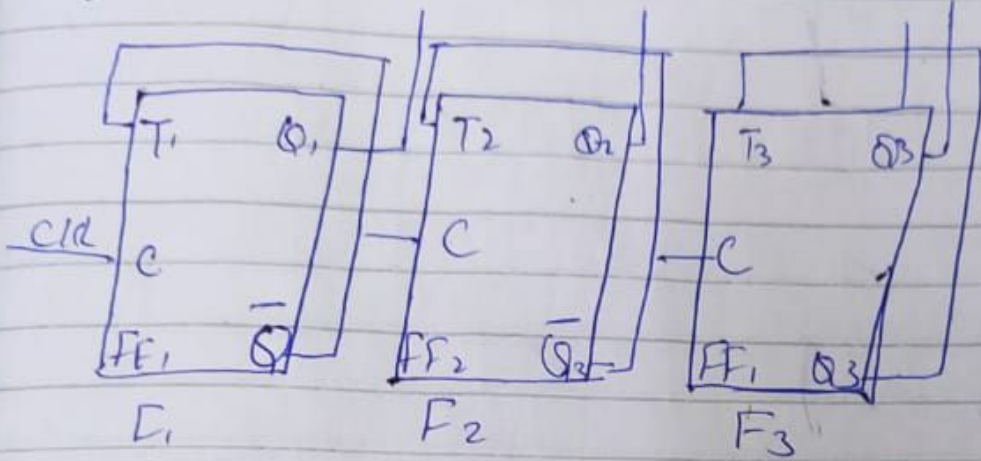
Q18



(9)

Q19)

$$Q_A = f/2 \quad Q_B = f/4 \quad Q_C = f/8$$



Here if the input frequency is 8 kHz then at given marks frequency will be as follows

$$Q_A = f/2 = 4 \text{ kHz}$$

$$Q_B = f/4 = 2 \text{ kHz}$$

$$Q_C = f/8 = 1 \text{ kHz}$$