Name Muhammad Ali Khan

RegNo 16550

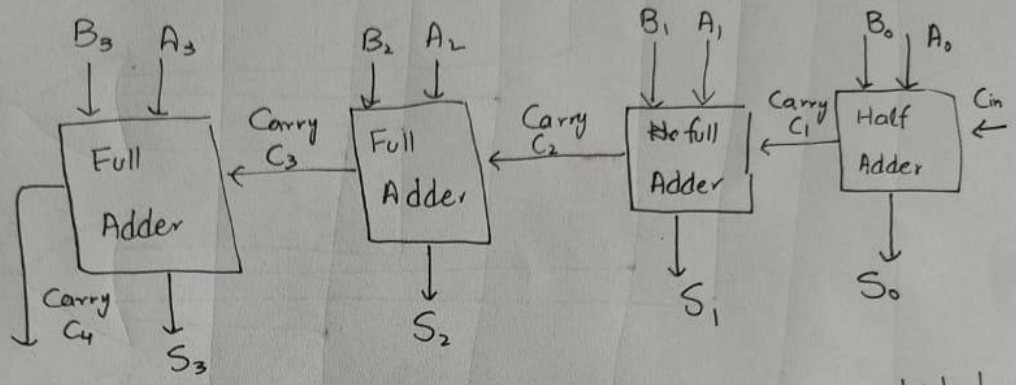
Dld Assignment

NAME: Muhammad Ali Khan

Reg No: 16550

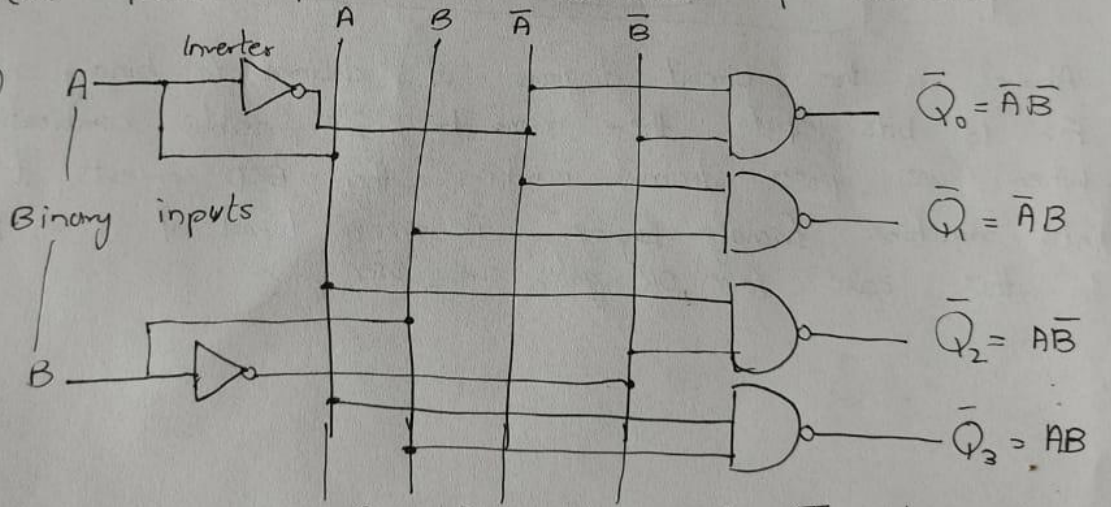
Q1

a)



The figure is 4-bit parallel binary adder which has two 4-bits inputs as A3A2A1A0 & B3B2B1B0.

b)



This consists of four AND gates. The binary 2 inputs A & B are decoded into one of 4 outputs, hence description of 2- to 4- binary decorder.

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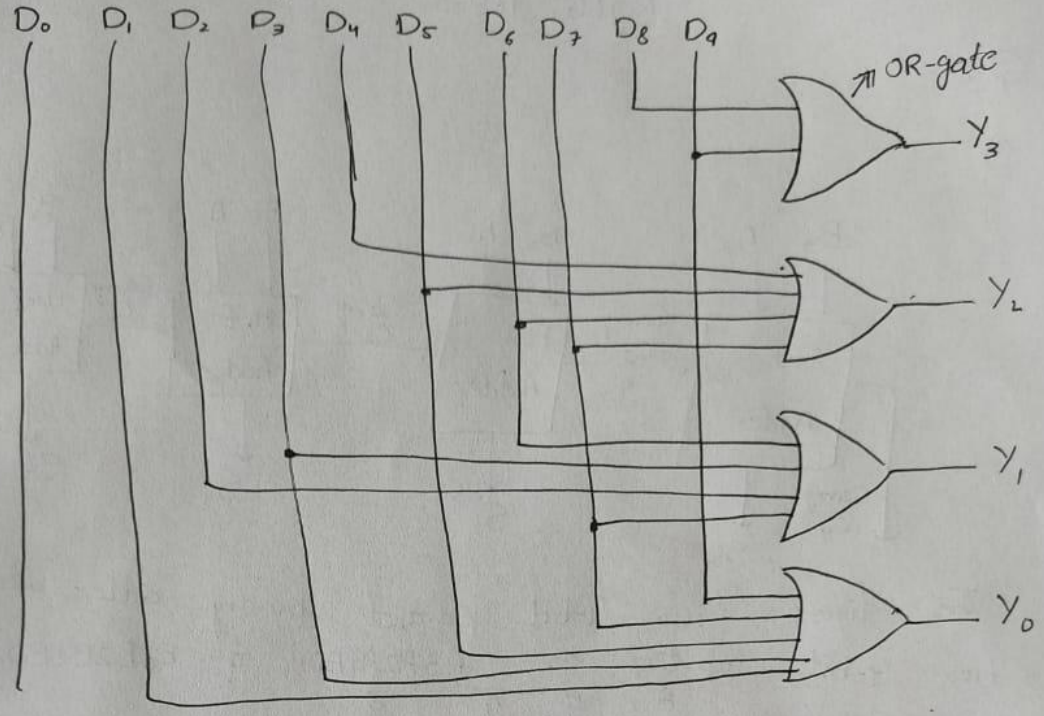
c)



Above is the circuit diagram of decimal to binary encoder. For 10 bits inputs there can be 2^{10} possible combinations. When we press decimal numbers then BCD converts it into machine friendly language i.e in terms of '0' & '1'. In this case four OR gates are used.

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Q2.

(a) In case of 4x1 Multiplexer.
When $S_0 = 0$ and $S_1 = 0$ then output is D_0.

S_0	S_1	Output
0	0	D_0

So output is 0

b)

S_0	S_1	Output
0	1	D_1

So the output is 1 as $D_1 = 1$

c)

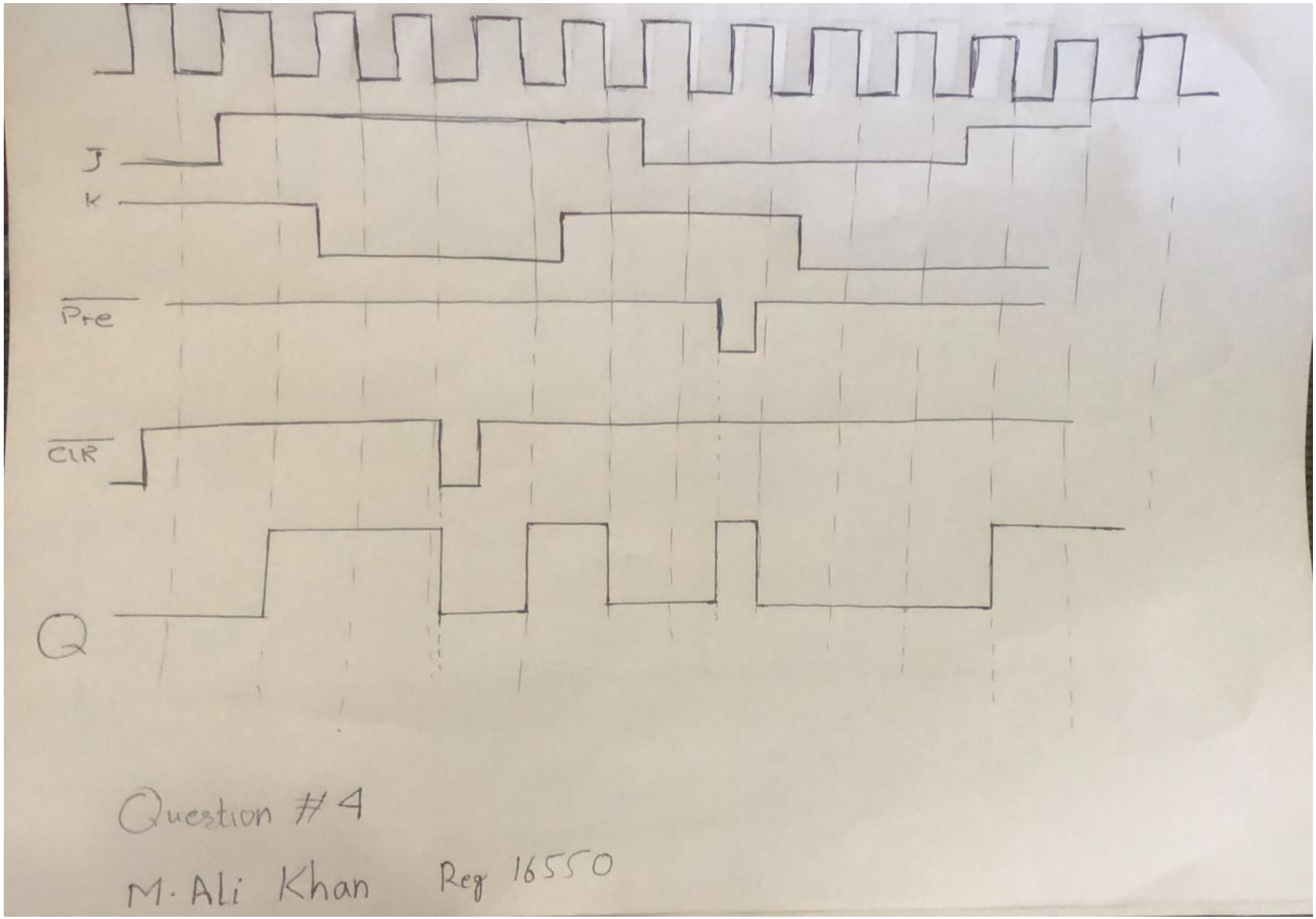
S_0	S_1	output
1	1	D_2

So the output is $D_2 = 0$

(d)

S_0	S_1	Output
1	0	D_3

So the output is $D_3 = 1$



Question #4

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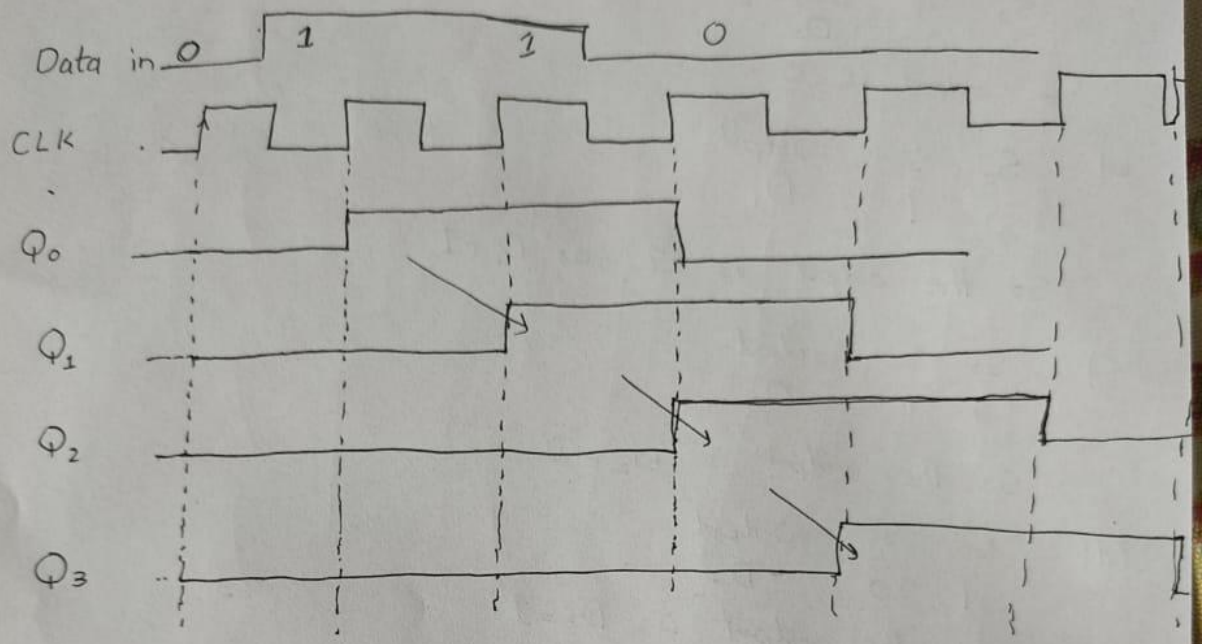
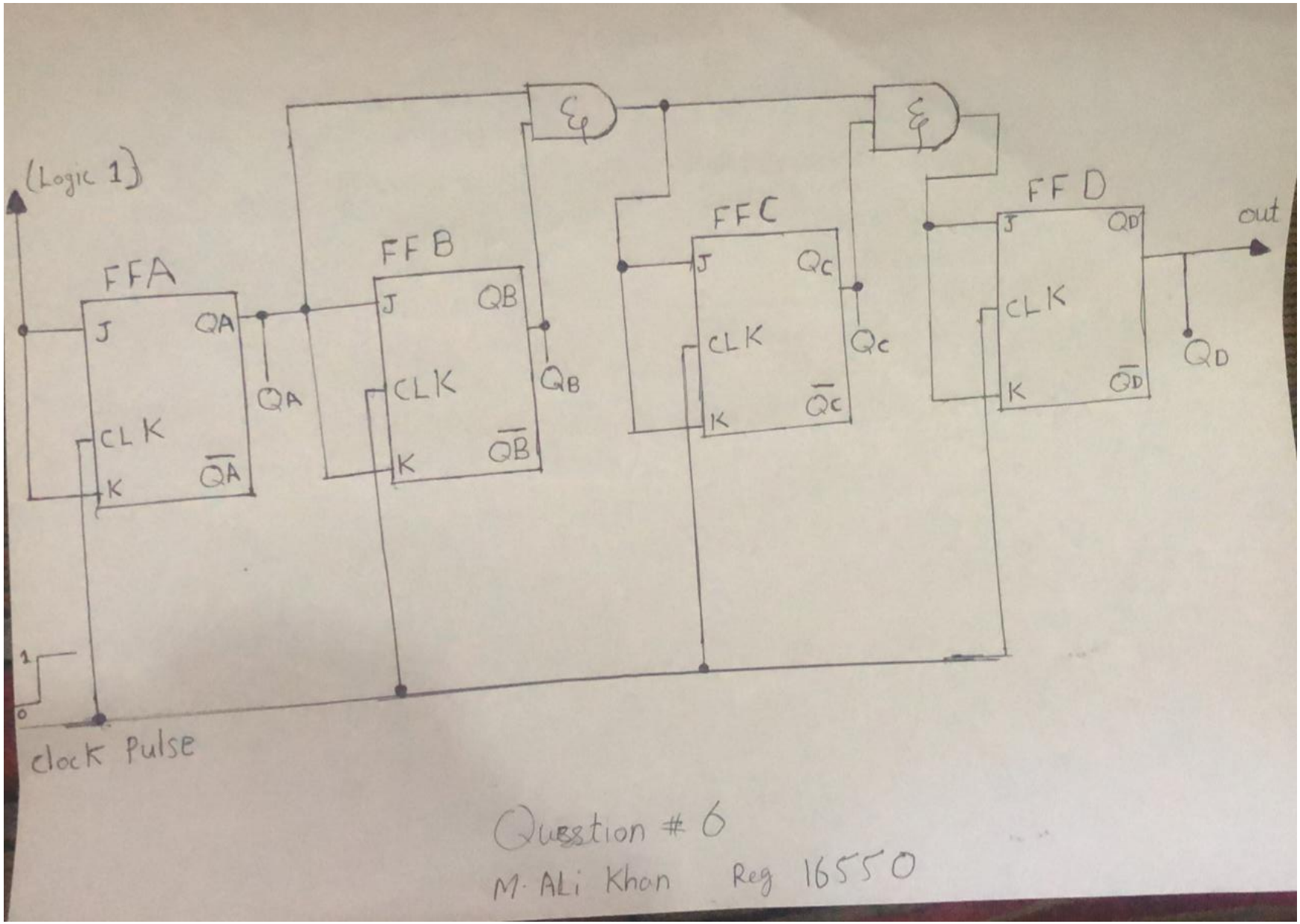
Q5:





Question # 6

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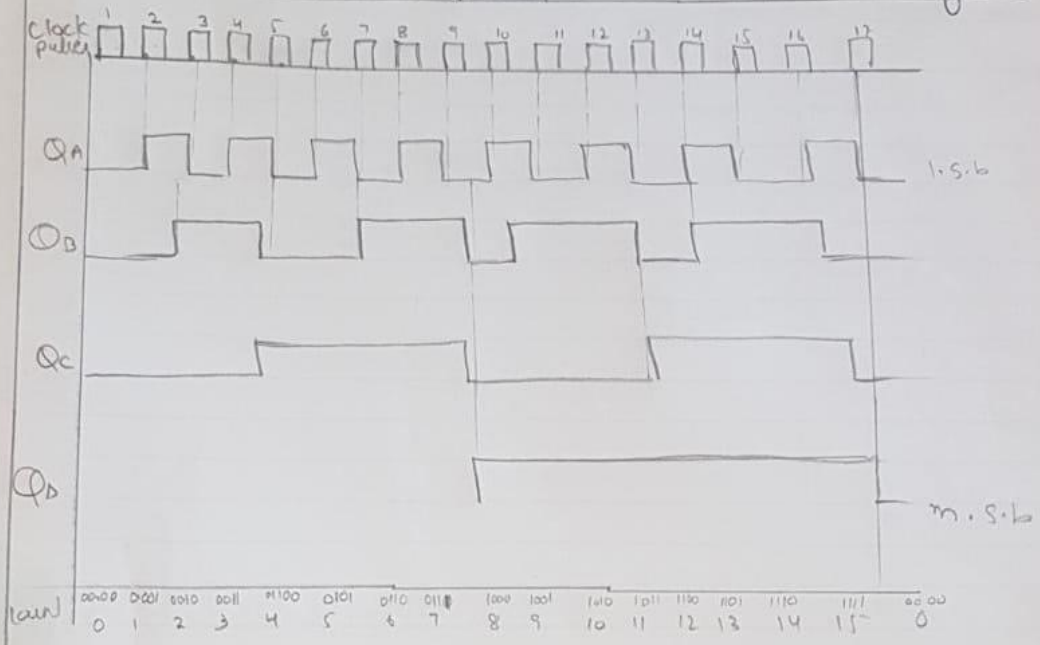
4-bit Synchronous Counter Waveform



Because This 4-bit synchronous counter counts sequentially on every clock pulse the resulting output count upwards from 0 (0000) to 15 (1111). Therefore, This type of counter is also known as 4-bit synchronous up counter

However, we can easily construct a bit 4-bit Synchronous Down counter by connecting