Question No 1

(A) Ans: Word:

The "natural" unit of organization of memory. The size of word is typically equal to the number of bits used to represent an integer

Addressable units:

In some, systems, the addressable unit is the word. However, many systems allow addressing at the byte level.

Unit of transfer:

For main memory, this is the

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number of bits read out of or written into memory at a time. The unit of transfer need not equal a word or an addressable unit.

b) Ans LRU:

For two-way set associative, this is easily implemented. Each line includes a USE bit. When a line is referenced, its USE bit is set to 1 and the USE bit of the other line in that set is set to 0. When a block is to be read into the set, the line whose

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USE bit is 0 is used.

LFU:

LFU could be implemented by associating a counter with each line. A technique not based on usage is to pick a line at random from among the candidate lines.

(c) Ans The SRAM address line is used to open or close a switch. The address line controls two transistors (T_5 and T_6). When a signal is applied to this line, the two transistors are switched on, allowing to read or write operation.

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For a write operation, the desired bit value is applied to line B, while its complement is applied to line B. This force the four transistors (T_1, T_2, T_3, T_4) into the proper states. For a read operation, the bit value is read from line B.

(d) Ans In typical organization of 16-Mbit DRAM, 4 bits are read or written at a time. logically, the memory array is organized as four square arrays of 2048 by 2048 elements. The elements of the array are connected by both

(5)

horizontal and vertical lines. Each horizontal line connects to the select terminal and vertical line connects to the Data-In/Sense terminal. A total of $\log_2 W$ lines are needed. 11 address lines are ~~selected~~ needed to select one of 2048 rows. These 11 lines are fed into row decoder, which has 11 lines of input and 2048 lines for output.

An additional 11 address lines select one of 2048 columns of 4 bits per column. 4 data lines are used for input and output of

4 bits to and from a data buffer. On input (write), the bit drivers of each bit line is activated for a 1 and 0 according to value of the corresponding data line. On output (read), the value of each bit line is passed through a sense amplifier and presented to the data line.

Because only 4 bits are read/written to this DRAM, there must be multiple DRAMs connected to the memory controller to read/write a word of data to the bus.

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(e) Ans: Reasons for DVD's greater capacity over CD.

The DVD's greater capacity is due to three differences from CDs:

1. Bits are packed more closely on a DVD. The spacing b/w loops of a spiral on a CD is 1.6 um and the minimum distance b/w pits along the spiral is 0.834 um. The DVD uses a laser with shorter wavelength and achieves a loop spacing of 0.74 um and a minimum distance b/w pits of 0.4 um

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The result of these two improvements is about a ~~DVD~~ seven-fold increase in capacity to about 4.7 GB.

2. The DVD employs a second layer of pits and lands on top of the first layer. A dual layer DVD has a semi-reflective layer on top of the reflective layer. This technique almost double the capacity of the disk, to about 8.5 GB.

3. The DVD-ROM can be two sided, whereas data are recorded only on on side of a CD.

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Question No 2

(a) EEPROM and Flash memory.

Ans EEPROM:

* EEPROM devices can erase any byte of memory at any time

* EEPROM uses Nor type memory.

* In micro-controllers, that's what you generally uses for holding configuration.

Flash memory:

* Flash memory can only erase an entire chunk

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or "sector" of memory at a time

* Flash memory uses Nand type memory.

* In micro-controller, it's generally used for firmware storage.

(b) Ans Hard Failure:

A hard failure is a permanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 switch erratically b/w 0 and 1. These may be manufacturing defects or harsh environmental abuse.

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Soft error:

A soft error is random, non destructive event that alters the contents of one or more memory cells without damaging the memory. Soft errors can be caused by power supply problems or alpha particles.

(c) Ans: Read:-

The traditional read mechanism exploits the fact that a magnetic field moving relative to a coil produces an electrical current in the coil. When the surface of disk passes under the head,

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it generates a current of the same polarity as the one already recorded. The structure of the head for reading is in this case essentially the same as for writing. Such single heads are used in floppy disk systems and in older rigid disk systems.

WRITE:-

The write mechanism exploits the fact that electricity flowing through a coil produces a a magnetic field. Electric pulse are sent to the write head ~~head~~, and the resulting magnetic.

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patterns are recorded on the surface below, with different patterns for positive and negative currents. The write head is in the shape of rectangular doughnut with a gap along one side and a few turns of conducting wire along the opposite side. An electric current in the wire induces a magnetic field across the gap which in turn magnetizes a small area of the recording medium.

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(d) Ans Parallel access:

All member disks participate in the execution of every I/O request. Typically, the spindles of the individual drives are synchronized so that each head is in the same position on each disk at any given time.

Independent access:

Each member disk operates independently, so that separate I/O requests can be satisfied in parallel.

(e) HD DVD and Blu-ray DVD:

HD DVD players have

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been much cheaper than Blu-ray machines, but Blu-ray discs have more storage space and more advanced protections against piracy. Both version deliver sharp resolution.

Blu-ray has 25 GB capacity and is more expensive.

HD DVD have 15 GB and is cheaper than Blu-Ray.

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Question No 3

(A) Ans There are 4 types of memory access methods.

(1) Sequential Access.

In this method, the memory is accessed in a specific linear sequential manner, like accessing in a single linked list. The access time depends on the location of the data.

(2) Random Access

In this method, any location of memory can be accessed randomly like accessing in Array. Main memory

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and some cache systems are random access.

(3) Direct Access:

In this method, the particular location of the memory can be accessed directly like accessing in Array. This method is a combination of above two access methods. Access time is variable.

(4) Associative Access:

In this method, a word is accessed rather than its address. This access method is a special type of random access method.

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(B) Ans Principle of Locality:

The principle of locality states that data in the vicinity of a referenced word are likely to be referenced in the near future.

OR

An implication of locality is that we can predict with reasonable accuracy what instruction and data a program will use in the near future based on its access in the recent past.

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(c) Ans: Possible approaches to cache coherency includes the following.

- Bus watching with write through:

Each cache controller monitors the address lines to detect write operations ~~to shared memory~~ to memory by other bus masters. If another master writes to a location in shared memory that also resides in the cache memory, the cache controller invalidates that cache entry. This strategy depends on the use of a write-through policy by all cache controllers

- Hardware transparency:

Additional hardware is used to ensure that all updates to main memory via cache are reflected. Thus, if one processor modifies a word in its cache, this update is written to main memory.

- Non-cacheable memory:

Only a portion of main memory is shared by more than one processor, and this is designated as non-cacheable. In such a system all access to shared memory are cache misses.

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(D) Ans There are two particular issues peculiar to SSDs that are not faced by HDDs:

1. SSD performance has a tendency to slow down as the device is used.
   - The entire block must be read from the flash memory and placed in a RAM buffer.
   - Before the block can be written back to flash memory the entire block of memory must be erased.
   - The entire block is now written back to the flash memory.

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7. Flash memory becomes unusable after a certain number of writes.

(e) Ans CD read and write operation

Read:

To read, a low-powered laser housed in an optical-disk player. The laser shines through the clear polycarbonate while a motor spins the disk past it. The intensity of the reflected light of the laser changes as it encounters a pit. Specifically, if the laser beam fall on a pit, which has a somewhat rough

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surface. The light scatters and a low intensity is reflected back. The land reflects back at higher intensity. The change b/w pits and lands is detected by a photo sensor and converted into the digital signal. The beginning or end of a pit represents a 1. when no change occurs, a 0 is recorded.

Write:-

Information is recorded in concentric tracks. With the simplest angular velocity system, the number of bits per track is constant. An increase

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in density is achieved with multiple zoned recording, in which the surface is divided into a number of zones, with zones farther from the center containing more bits than zones closer to the center.

Question No 4

(a) Sol:-

Suppose 95% of the memory accesses are found in level 1. Then the average time to access a word can be expressed as

$$(0.95)(0.01\mu s) + (0.05)(0.01\mu s + 0.1\mu s)$$
$$= 0.0095 + 0.0055$$

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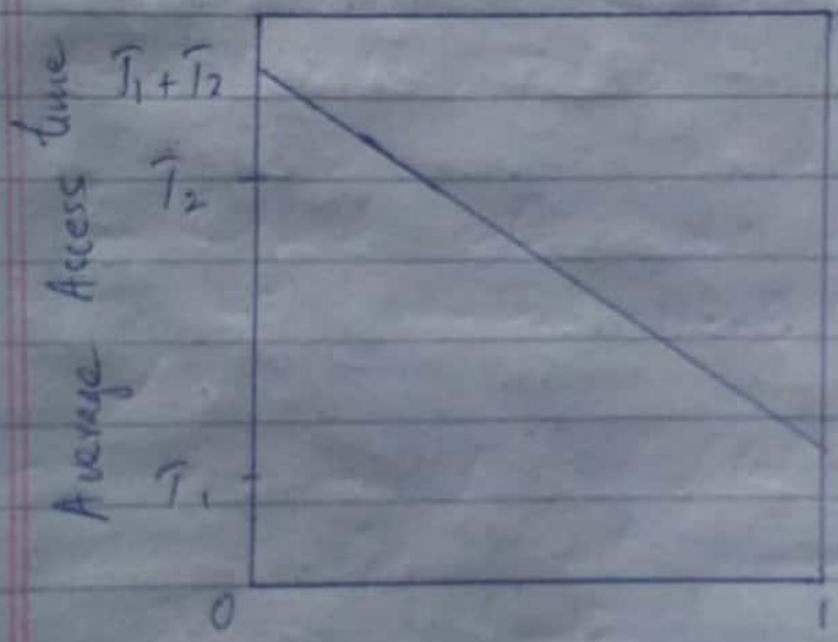
$= 0.015\ \mu s$

The average access time is much closer to 0.01 μs than to 0.1 μs, as desired.



(b) Sol:

Total block in the cache = 8Kb / 16Kb

$= 2^3 \times 2^{10} / 2^4 = 2^9 = 512$

Number of set = number of block in cache / 2

Number of set in = 512/2

No of set in cache = 256

No of set in cache = 2^8

No of set = 8

Size block = 16 = 2^4

Size of memory = $2^6 \times 2^{20} = 2^{66}$

Tag = size of memory - set - size of block

Tag = 26 - 8 - 4

Tag = 14

Tag	set	Size of block
14	8	4

Tag set and word.

Tag (14) / set (13) / word (2)

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(c) Sol.

$M = 8$

$2^r - 1 >= k + m$

$2^4 - 1 >= 4 + 8$

$15 >= 12$

1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	1	1	0	0	1	0	0	1	0

The check bits are in a bit numbers 1, 2, 0, 4 and 8

- Check bit 4 calculated by values in bit numbers: 5, 6, 7 and 12.
- Check bit 2 calculated by values in bit numbers: 3, 6, 7, 10 and 11
- Check bit 1 calculated by values in Bit numbers: 3, 5, 7, 9, 10 and 11.

Thus the check bits are: 1011

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