

DIGITAL LOGIC DESIGN

Synchronous Counter

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LAB# 11

Synchronous Counter

AIM:

Realization of 3-bit synchronous counter design.

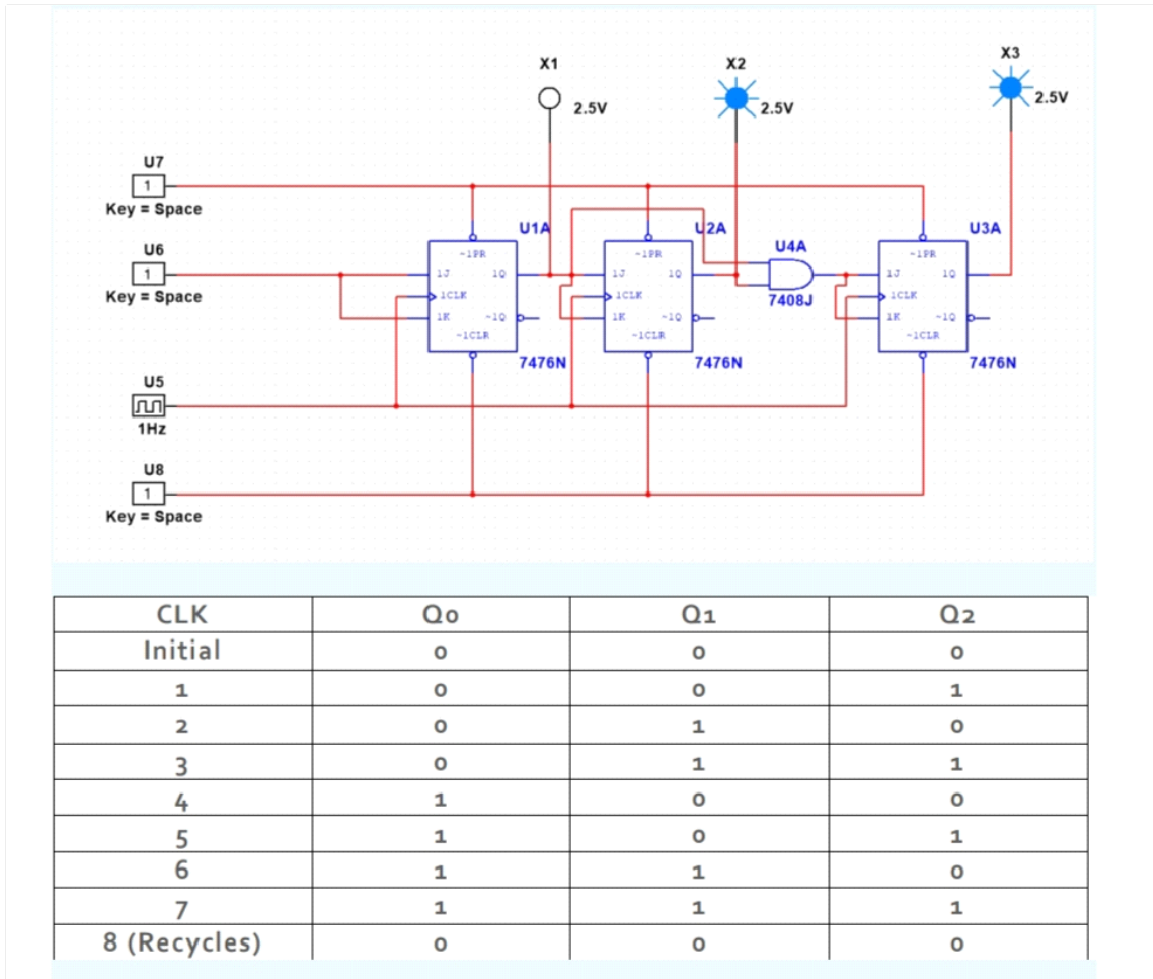
PROCEDURE:

Connections are made as per circuit diagram.

Clock pulses are applied one by one at the clock I/P and the O/P is observed at QA, QB & QC for IC 7476.

Verify the Truth table.





CONCLUSION:

o3-bit synchronous counter has been implemented and verified using ICs.

