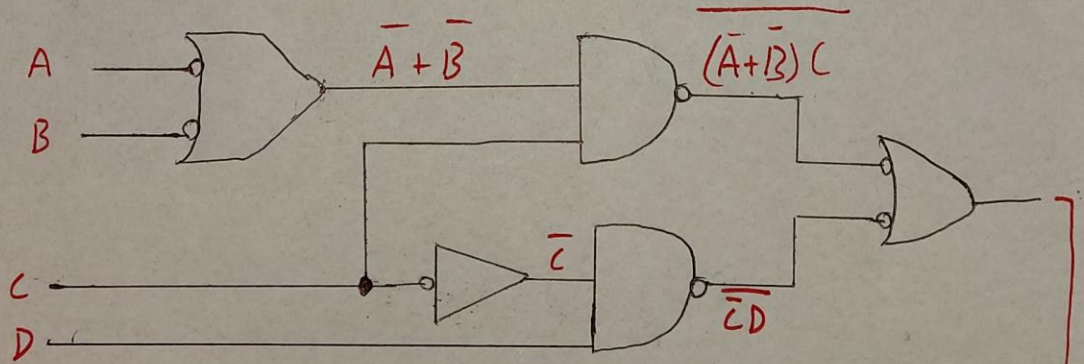
DLD Final Paper

M.Abbas 13063 BSSE-B

Q1) DRaw a logic circuit using the input (A, B, C, D) and output (x) waveforms in Fig 01

Sol:- The output expression for the circuit is developed in the SOP form indicates that output is High when A is low and C is High or when B is low and C is High or when C is Low and D is High.



$$x = (\bar{A}+\bar{B})C + \bar{C}D = (\bar{A}+\bar{B})C + \bar{C}D = \bar{A}C + \bar{B}C + \bar{C}D$$

(Q2) For the 4-input multiplexer, data inputs are:
$D_0 = 0$, $D_1 = 1$, $D_2 = 0$, $D_3 = 1$

Find output y if

$S_0 = 1$	$S_1 = 0$
$S_0 = 0$	$S_1 = 1$
$S_0 = 1$	$S_1 = 1$
$S_0 = 0$	$S_1 = 0$

Sol:-

A 4x1 multiplexer has 4 input lines (D_0, D_1, D_2, D_3) two select input (S_0 and S_1) and one output line Y

if	$S_1 S_0 = 00$	then	$Y = D_0$
if	$S_1 S_0 = 01$		$Y = D_1$
if	$S_1 S_0 = 10$		$Y = D_2$
if	$S_1 S_0 = 11$		$Y = D_3$

Data input		output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Q3

Sol:-

Full adder 4	Full adder 3	Full adder 2	Full adder 1
$G_4 = A_4 B_4$	$G_3 = A_3 B_3$	$G_2 = A_2 B_2$	$G_1 = A_1 B_1$
$P_4 = A_4 + B_4$	$P_3 = A_3 + B_3$	$P_2 = A_2 B_2$	$P_1 = A_1 B_1$

Full adder 1:

$$C_{out} = G_1 + P_1 C_{in1}$$

Full adder 2:

$$C_{in2} = C_{out1}$$

$$C_{out2} = G_2 + P_2 C_{in2} = G_2 + P_2 C_{out1} = G_2 + P_2 (G_1 + P_1)$$
$$= G_2 + P_2 G_1 + P_2 P_1 C_{in1}$$

Full adder 3

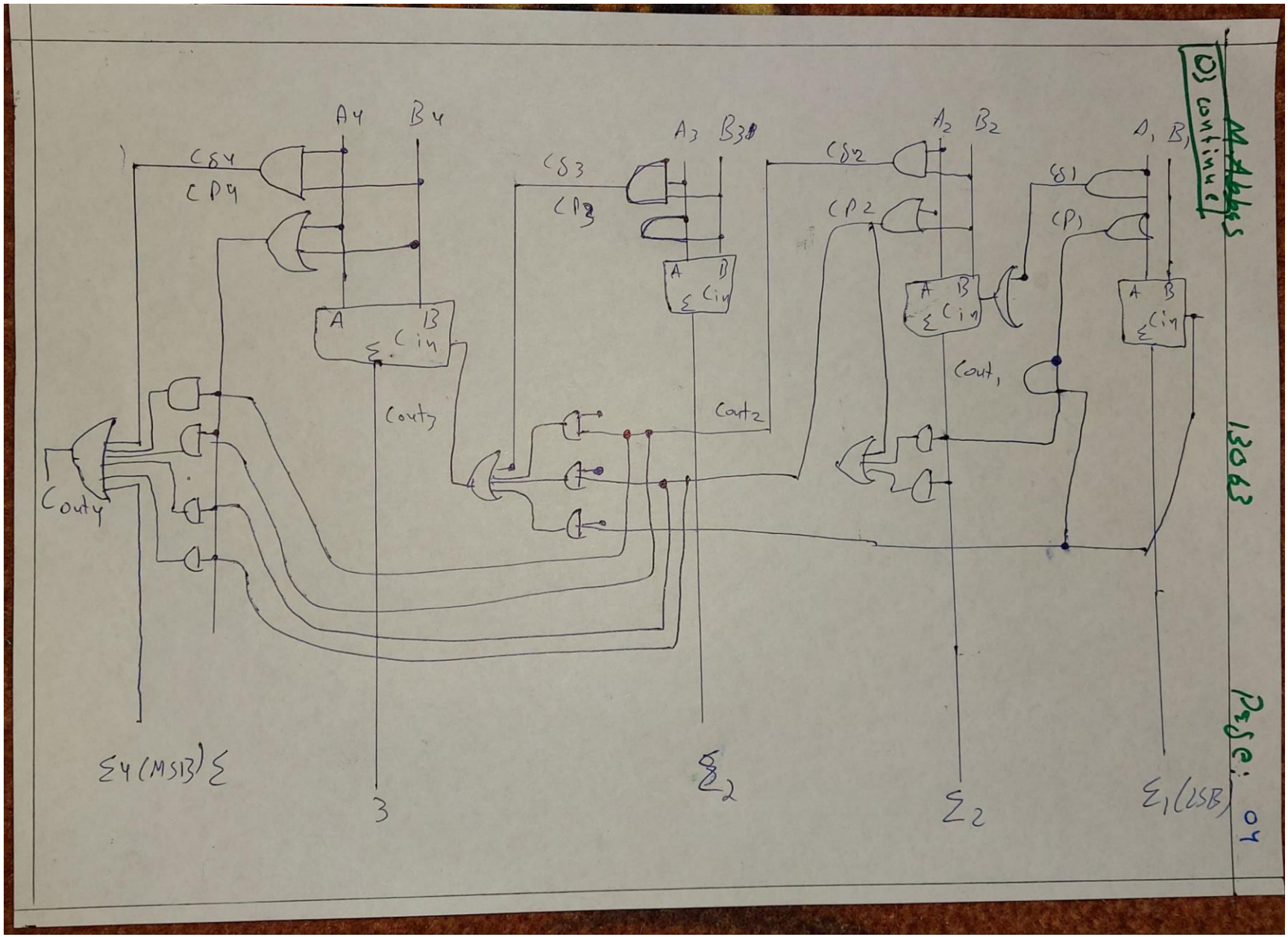
$$C_{in3} = C_{out2}$$

$$C_{out} = G_4 + P_4 C_{in4} = G_4 + P_3 C_{out2} = P_3 (G_2 + P_2 G_1 C_{in1}) = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 C_{in1}$$

Full adder 4

$$C_{in4} = C_{out3}$$

$$C_{out4} = G_4 + P_4 C_{in4} = G_4 + P_4 C_{out3}$$
$$= G_4 + P_4 (G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 C_{in1})$$
$$= G_4 + P_4 G_3 + P_4 P_3 G_2 + P_4 P_3 P_2 G_1 + P_4 P_3 P_2 P_1 C_{in1}$$



(c) continued

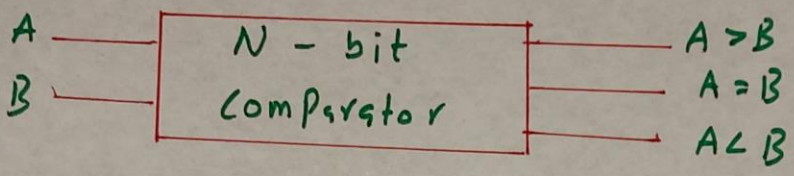
M. Abbas

130963

Page: 04

Q4) Determine the A=B, A>B, and A<B outputs for the input numbers shown on the comparator.

Sol:-



A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Truth table

→ Truth Table

From the above↑ expressions for each out put can be exprosed as.

A > B : AB'

A < B : $A'B$

A = B : $A'B' + AB$

Now we can derive the formula.

$(A<B)+(A>B) = A'B + AB'$

Taking compliment both sides

P.T.O

Q4 continue

$$((A<B)+(A>B))' = (A'B)+AB')'$$

$$((A<B)+(A>B))' = (A'B')(AB')'$$

$$= (A+B)(A'+B)$$

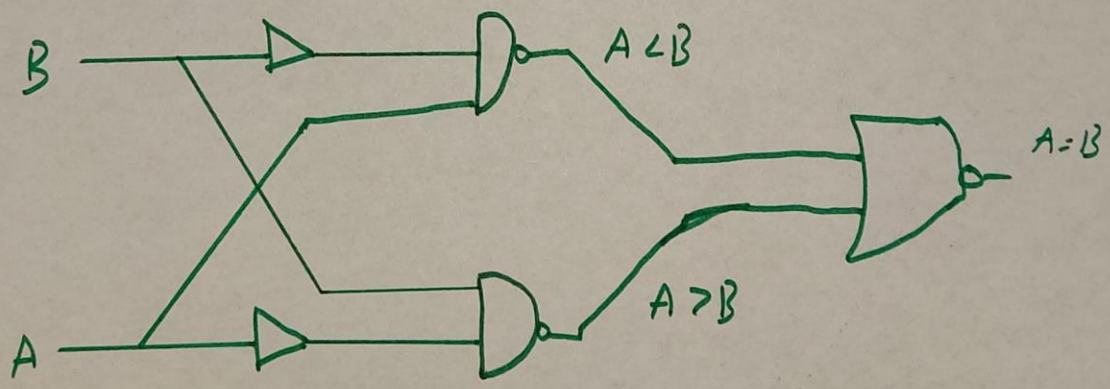
$$= (AA'+AB+A'B+BB')$$

$$= (AB+A'B')$$

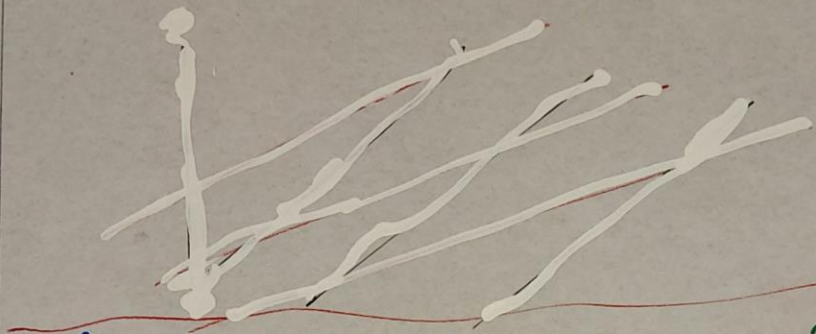
Thus

$$((A<B)+(A>B))' = (A=B)$$

Logic circuit for this comperator



Q5) Convert [redacted] Gray code words to binary: 1011



Sol:-

b_3	b_2	b_1	b_0
1	0	1	1
+	+	+	
1	1	0	1
1	1	0	0
δ_3	δ_2	δ_1	δ_0

Gray code

$\delta_3 = b_3$

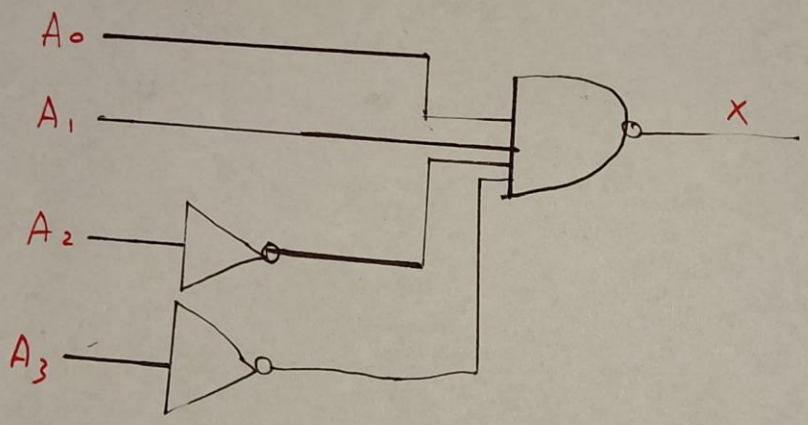
$\delta_2 = b_2 + b_3$

A	B	$y = AB' + A$ (A + B)
0	0	0
0	1	1
1	0	1
1	1	0

Q6) Draw and explain 4-bit active low decorder.

Sol:-

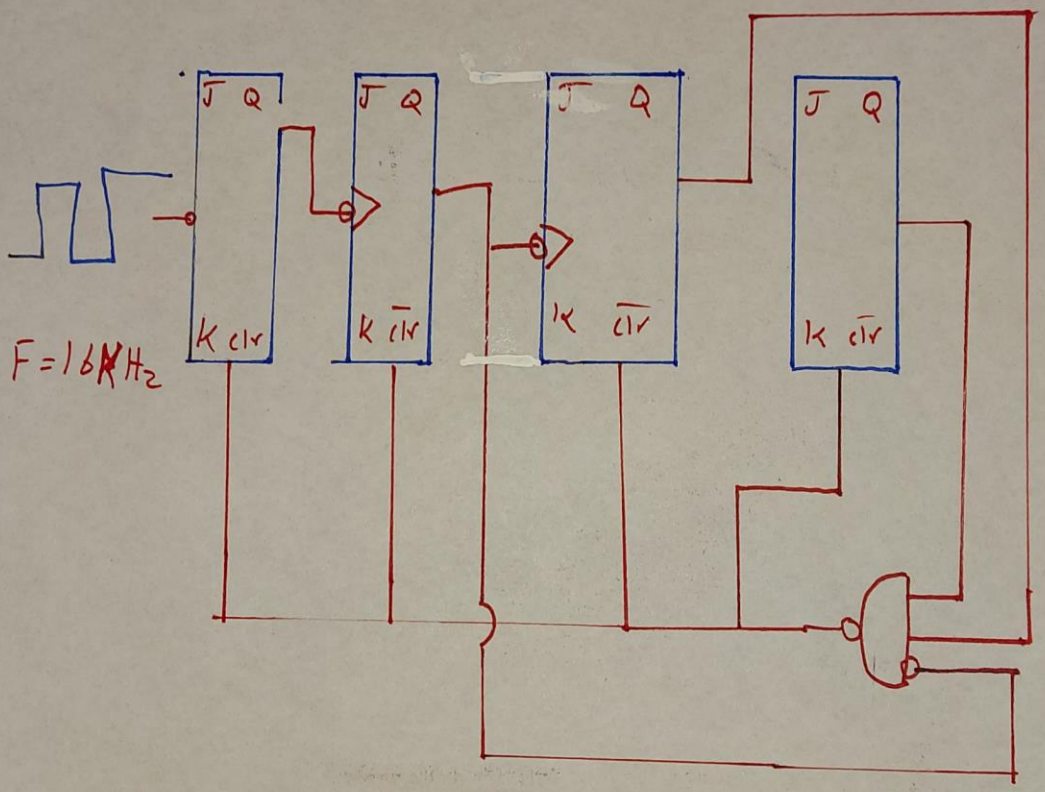
A Decorder is a logic circuit that detects the Presence of a specific combination of bits at its input. Two simple decorders that detects the Presence of binary code 0011 are shown. It has an Active low output.



Active low decorder

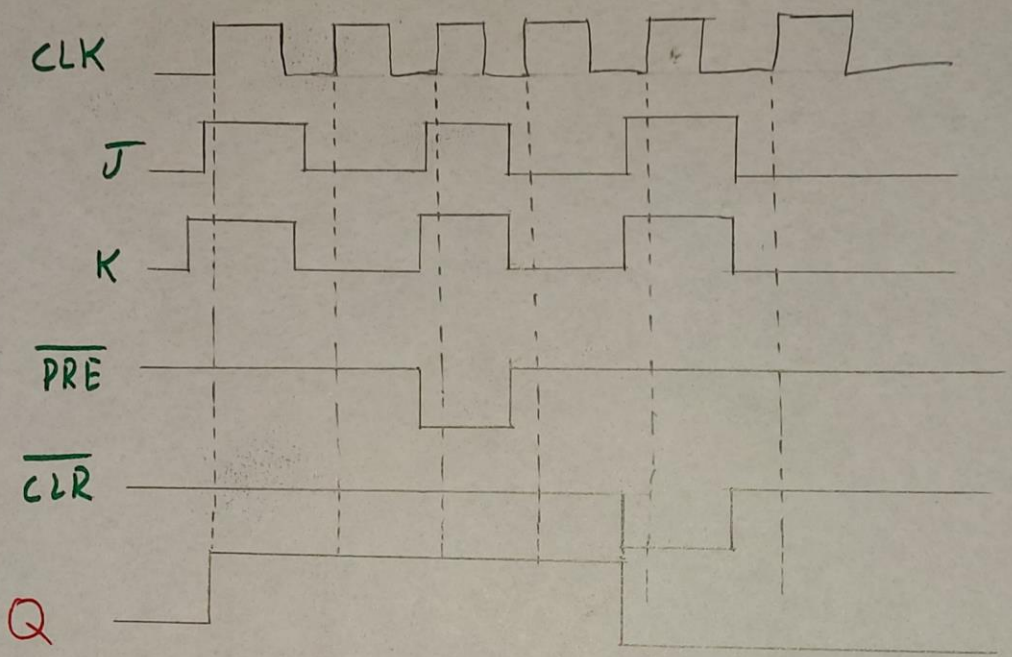
Q7) Draw and explain the logic diagram for frequency divide.....

sol:-



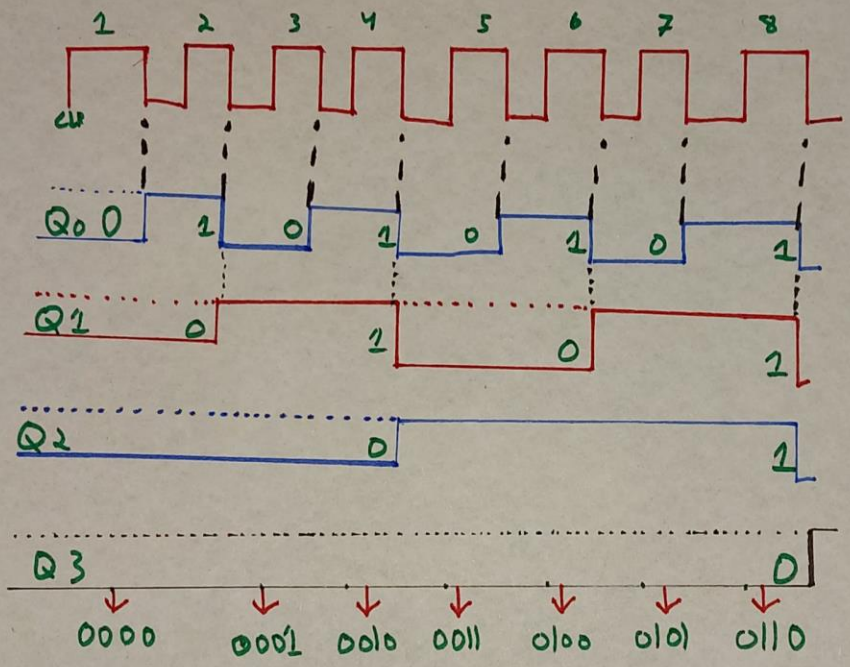
Explanation:- It can be seen from the frequency waveforms above, that by "Feeding back" the output from Q to the input J, the output pulse Q have a frequency that are exactly one half that of the clock frequency.

Q8



Q9

Sol :-


1 2 3 4 5 6 7 8
CLK
Q0 0 1 0 1 0 1 0 1
Q1 0 1 0 1
Q2 0 1
Q3 0
0000 0001 0010 0011 0100 0101 0110