:: FINAL TERM ASSIGNMENT ::

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Subject: Computer Architecture

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QUESTION: (a)

Discuss the concept of word, addressable units, and unit of transfer for internal memories.

ANSWER:—

FOR INTERNAL MEMORY:—

For internal memory, the unit of transfer is equal to the number of electrical lines into & out of memory module. This may be equal to the word length, but is often larger, such as 64, 128 or 256 bits. To clarify this point, consider these related concepts for internal memory:—

→ **WORD:—** The "natural" unit of organization of memory. The size of a word is typically equal to the number of bits used to represent an integer & to the instruction length. Unfortunately, there are many exceptions. For example, the CRAY C90 has a 64-bit word length but uses a 46-bit integer representation. The Intel x86

has a wide variety of instruction lengths, expressed as multiples of bytes, and a word size of 32 bits.

ADDRESSABLE UNITS:— In some systems, the addressable units is the word. However many systems allow addressing at the byte level. In any case, the relationship between the length in bits A of an address and the number N of addressable units is $2^A = N$

UNIT OF TRANSFER:— For main memory, this is the number bits read out of or written into memory at time. The unit of transfer need not equal a word or an addressable unit. For external memory, data are often transfered in much larger units than a word, and these are referred to as blocks.

→ **FOR EXTERNAL MEMORY:—** Usually a block which is much larger than a word.

→ **ADDRESSABLE UNIT:—** Smallest location which can be uniquely addressed

Word intentionally
Cluster on M$ disks.

QUESTION: (b)

How least recently used (LRU) and less frequently used (LFU) replacement algorithms are implemented for a cache memory with two-way set associative mapping?

ANSWER:-

LEAST RECENTLY USED (LRU):-

Replace the block in the set that has been in the cache longest with no reference to it. For two-way set associative, this is easily implemented. Each line includes a USE bit. When a line is refferenced its USE bit is set to 1 and the USE bit of other line in that set is set to 0. When a block is to be read into the set, the line whose USE bit is 0 is used. Because we are assuming that more recently used memory locations are more likely to be referenced. LRU should give

the best hit ratio. LRU is relatively easy to implement for a fully associative cache. The cache mechanism maintains a separate list of indexes to all the lines in the cache. When a line is referenced, it moves to the front for the list. For replacement, the line of the back of the list is used. Because of its simplicity of implementation LRU is the most popular replacement algorithm.

Least Frequently Used (LFU):-

LFU could be implemented by associating a counter with each line. A technique not based on usage (i.e not LRU, LFU, FIFO or some variant) is to pick a line at random from among the candidate lines. Simulation studies have showed that random replacement provide only slightly inferior performance to an algorithm based on usage.

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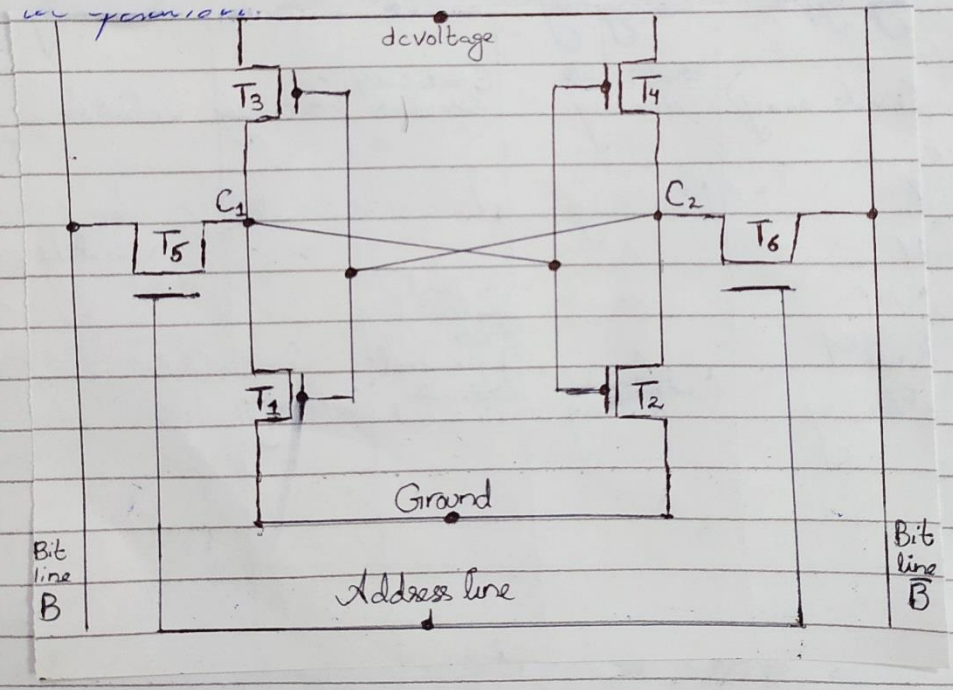
QUESTION: (c)

How read and write operations are performed in SRAM cell?

ANSWER:-



This figure is a typical SRAM structure for an individual cell. Four transistors (T_1, T_2, T_3, T_4) are cross connected in an arrangement that produces a stable logic state. In logic state 1, point C_1 is high and C_2 point is low; in this state, T_1 and T_4 are off and T_2 and T_3 are on. In logic state 0, point C_1 is low and point C_2 is high; in this state the T_1 and T_4 are on and T_2 and T_3 are off. Both states are stable as long as the direct current (dc) voltage is applied. Unlike the DRAM, no refresh is needed to retain data. The SRAM address line is used to open or close a switch. The address line controls two transistors (T_5 and T_6). When a signal is applied to this line, the two transistors are switched on, allowing a read or write operation.

For the write operation, a voltage signal is applied to the bit line; a high voltage represents 1 and a low voltage represents 0. A signal is then applied to the address line, allowing a charge to be transferred to the capacitor.

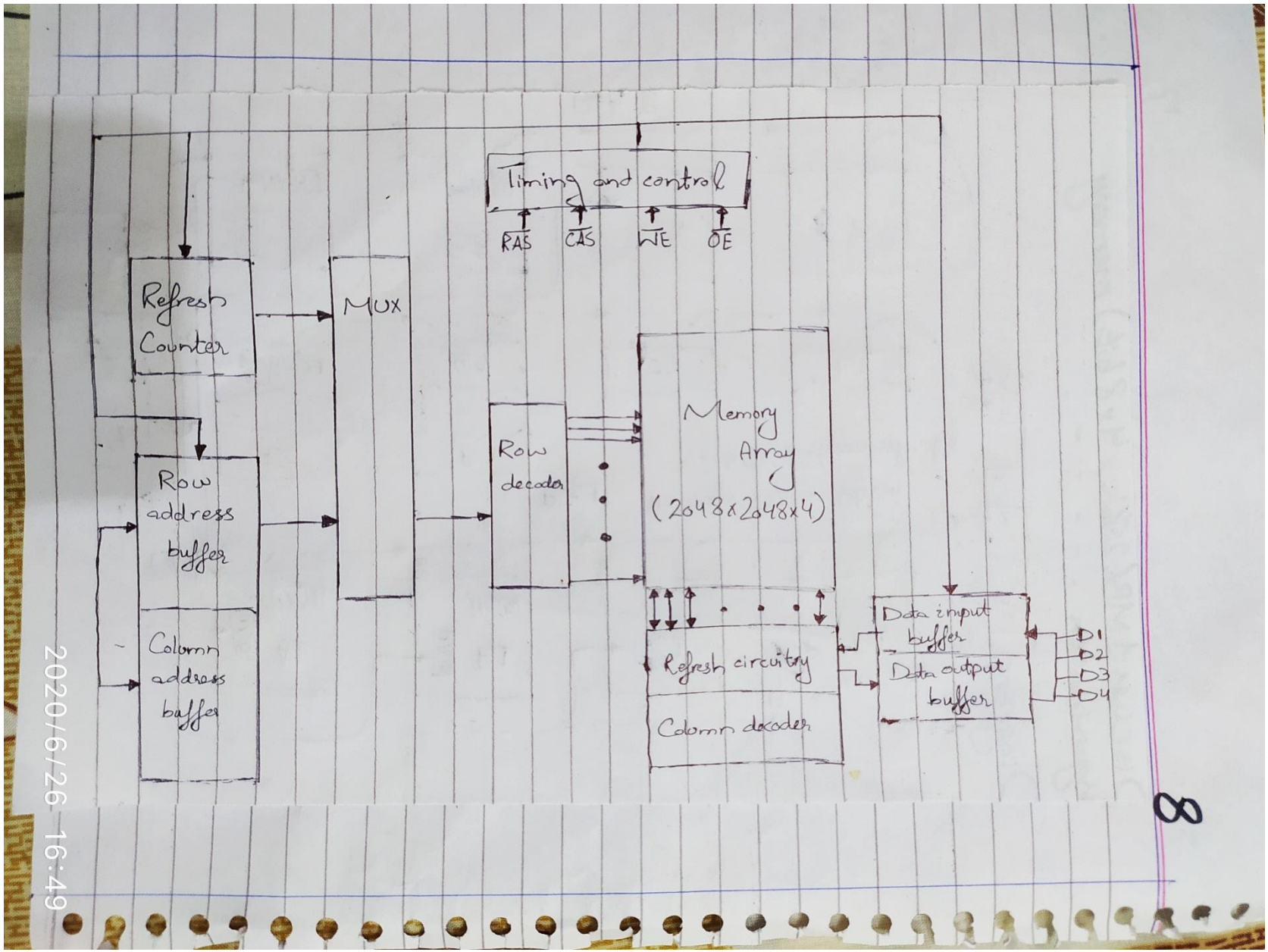
For the read operation, when the address line is selected, the transistor turns on & the charge stored on the capacitor is fed out onto a bit line & to sense amplifier. The sense amplifier compares the capacito voltage to a reference value & determines if there the cell contains a logic 1 or logic 0. The readout from the cell discharges the capacitor, which must be restored to complete the operation.

QUESTION: (d)

Discuss the 16-Mbit DRAM (4M x 4) organization in detail.

ANSWER:-

Diagram



In the case of this diagram:-

- 4 bits are read or written at a time
- Memory array is organized as four arrays of 2048 by 2048 elements;
- Address lines supply the address of the word to be selected;
- log 2W lines are needed,
- E.g.; 11 address lines are needed to select one of 2048 rows;
- These lines are fed into a row decoder,
- Decoder activates a single single line of memory.
- The same procedure is applied to select columns,
- Note that there are only 11 address lines (A0 - A10)
- Half the number you would expect for a 2048 - 2048 array.
- First, a row address select (RAS) signal is emitted.
- to define the row address of the array
- Second a column address select (CAS) signal is emitted.
- to define the column address of array
- Write enable (WE) signal
- specifies that a write operation is to be performed.

- Output enable (OE)
- signal specifies that a read operation is to be performed,
- Refreshing technique
- Refresh counter: step through all of the rows values;
- For each line
- Memory row is chosen
- RAS line is activated
- Data are read out and written back into the same location.

QUESTION: (e)

What are the reasons for DVD's greater capacity over CD?

ANSWER:-

The DVD's greater capacity is due to three differences from CD's.

1. Bits are more packed closely on a DVD. The spacing between loops of a spiral on a CD is 1.6 mm & the

minimum distance between the pits along the spiral is 0.834 mm. The DVD uses a laser with shorter wavelength & achieves a loop spacing of 0.74mm & a minimum distance between the pit of 0.4mm. The result of these two improvements is about a seven fold-increase in capacity, to about 4.7GB

2.) The DVD employs a second layer of pits & lands on top of first layer. A dual layer DVD has a semi reflective layer on top of the reflative layer, & by adjusting focus, the lasers in DVD drives can read each layer separately. This technique almost doubles the capacity of the disk, to about 8.5 GB. The lower reflectivity of the second layer, limits it's storage capacity so that a full doubling is not achieved.

3.) The DVD ROM can be two sided, whereas data are recorded on only one side of a CD. This brings total capacity upto 17 GB. As with the CD, DVDs come in writeable as well as read-only versions.

QUESTION: 2

Differentiate each of the following in detail.

Part: (a)

EEPROM and flash memory.

ANSWER:-

IN EEPROMs: -

The chip doesn't have to remove to be written.

The entire chip doesnot have to be completely erased to change a specific portion of it.

Changing the contents does not require additional dedicated equipment.

Instead of using UV Right, you can return the electrons in the cells of an EEPROM to normal with the localized application of an electric field to each cell. This erases the targeted cells of the EEPROM, which can then be rewritten. EEPROM are changed byte.

At a time, which makes them versatile but slow, In fact, EEPROM chips are too slow to use in many products that make quick change to the data stored on the chip.

⇒ FLASH MEMORY :-

Manufacturers responded to this limitation with Flash memory, a type of EEPROM that uses in-circuit wiring to erase by applying an electrical field to the entire chip or to predetermined sections of the chip called blocks. Flash memory works much faster than traditional EEPROMs because it write data in chunks, usually 512 bytes in size instead of 1 byte at a time.

Part (b)

Hard failure and soft error in semiconductor memories.

Answer:-

HARD FAILURES-

A hard failure is a permanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch between 0 and 1. Hard errors can be caused by harsh environmental abuse, manufacturing defects, and wear.

SOFT ERRORS:-

A soft error is random, nondestructive event that alters the contents of one or more memory cells without damaging the memory. Soft errors can be caused by power supply problems or alpha particles.

These particles result from radioactive decay & are distressingly common because radioactive nuclei are found in small quantities in nearly all materials. Both hard & soft errors are clearly undesirable and most modern main memory system include logic for both detecting & correcting soon.

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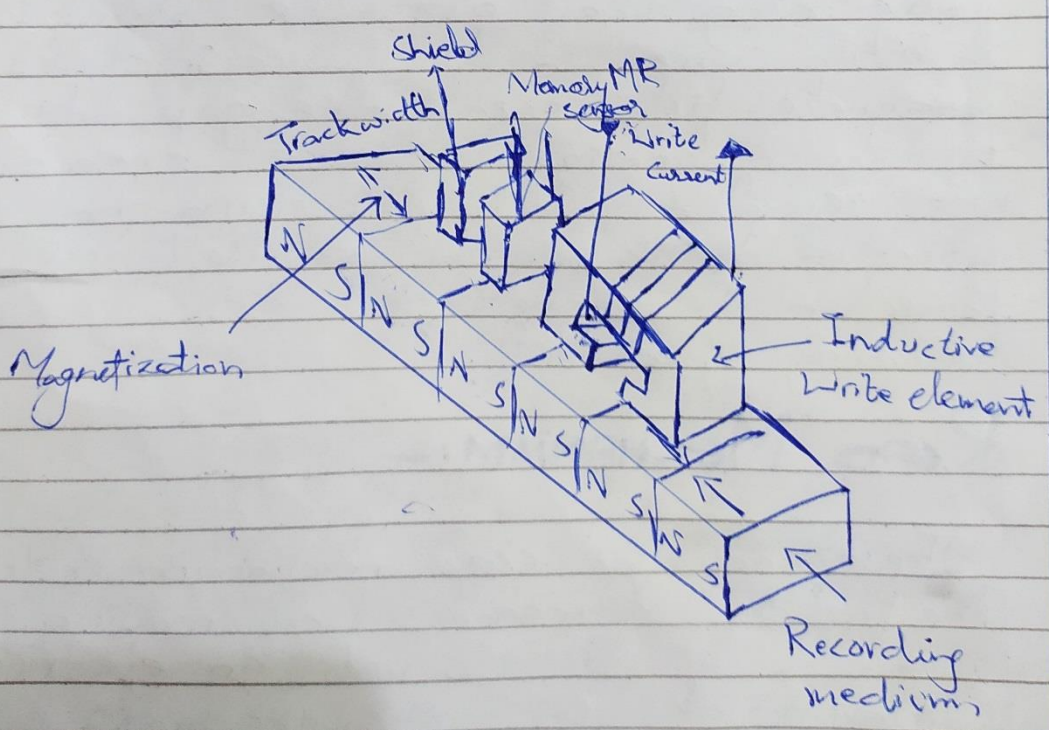
Part: (c)

Read and write mechanism for magnetic disk.

ANSWER:-

WRITE MECHANISM :-



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The write mechanism exploits the fact that electricity flowing through a coil produce a magnetic field. Electric pulses are sent to the write head, and the resulting magnetic patterns are recorded on the surface below, with different patterns for positive and negative currents. The write head itself is made of easily magnetizable material & is in the shape of a rectangular doughnut with a gap along one side and few turns of conducting wire along the opposite side. An electric current in the wire induces a magnetic field across the gap, which in turn magnetizes a small area of the recording medium. Reversing the direction of the current reverses the direction of magnetization on the recording medium.

READ MECHANISM:—

The traditional read mechanism exploits the fact that a magnetic field moving relative to a coil produces an electrical current in the coil. When the surface of

the disk rotates under the head, it generates a current of the same polarity as the one already recorded. The structure of the head for reading is in this case essentially the same as for writing & therefore the same head can be used for the both. Such single heads are used in floppy disk systems & in older rigid disk systems.

Contemporary rigid disk systems use a different read mechanism, requiring a separate read head positioned for convenience close to the write head. The read head consists of partially shielded magneto resistive (MR) sensor. The MR material has an electrical resistance that depends on the direction of the magnetization of the medium moving under it. By passing a current through the MR sensor, resistance changes are detected as voltage signals. The MR design allows higher frequency operation, which equates to greater storage densities & operating speeds.

Part: (d)

Parallel access & independent access Raid schemes.

Answer:-

Parallel Access Raid Schemes	Independent Access Raid Schemes
In Parallel access Raid schemes all member disks participate in the execution of every I/O request. Typically, the spindles of the individual drives are sychronized so that each disk head is in the same position on each disk at any given time	In Independent access Raid scheme, each member disk operates independently, so that separate I/O requests can be satisfied in Parallel!

Part (e)

HD, DVD & Blu-ray DVD

Answer:-

→ The pit on an HD-DVD are different size than on Blu-ray Disc, which means that the pits on the disc must be read by a laser of specific light wavelength.

→ A HD-DVD has a 15GB per layer storage capacity, while a Blu-ray Disc has 25 GB per layer storage capacity.

→ There is also a difference in how disc menus are constructed and navigated.

→ HD DVD discs also have a different surface layer (the clear plastic layer on the surface of the data - what you get fingerprints and scratches on) from Blu-ray discs. HD DVD use a 0.6 mm thick surface layer, the same as DVD, while Blu-ray has a much smaller 0.1 mm layer to help enable the laser to focus with that 0.85 aperture. This leads to higher costs for Blu-Ray discs.

→ The Blu-ray disc has a higher track ~~pitch~~ (the single thread of data that spirals from the inside of the disc all the way out) it can hold more pits (microscopic 0s & 1s) on the same disc as HD DVD even with a laser of the same wavelength. The differing track pitch of the Blu-ray disc makes it pickup aperture differ, however - 0.65 for HD DVD vs. 0.85 for Blu-ray thus also making the two pickups technically incompatible despite using lasers of the same type.

QUESTION: 3

Write a note on each of the following.

Part (a)

Memory access methods.

ANSWER:-

SEQUENTIAL ACCESS:-

Memory is organized into units of data called records. Access must be made in a specific linear sequence. Stored addressing information is used to separate records and assist in the retrieval process. A shared read-write mechanism is used, and this must be moved from its current location to the desired location, passing & rejecting each intermediate record. Thus, the time to access an arbitary record is highly variable. Tape units, are sequential access.

DIRECT ACCESS:-

As with sequal access, direct access involves a shared read-write mechanism. However individual block or records have a unique address based on physical location. Access is accomplished by direct access to reach a general vicinity plus sequential searching, counting, or waiting to

reach the final location. Again, access time is variable. Disk units are direct access.

RANDOM ACCESS:—

Each addressable location in memory has a unique, physically wired-in addressing mechanism. The time to access given in location ~~in memory may~~ ~~[illegible]~~ is independent of the sequence of prior accesses & is constant. Thus, any location can be selected at random & directly accessed. Main memory and some cache system are random access.

ASSOCIATIVE:—

This is a random type of memory that enables the one to make a comparison of desired bit locations within a word for a specified match, and to do this for all words simultaneously. Thus, a word is retrieved based on a portion of its contents rather

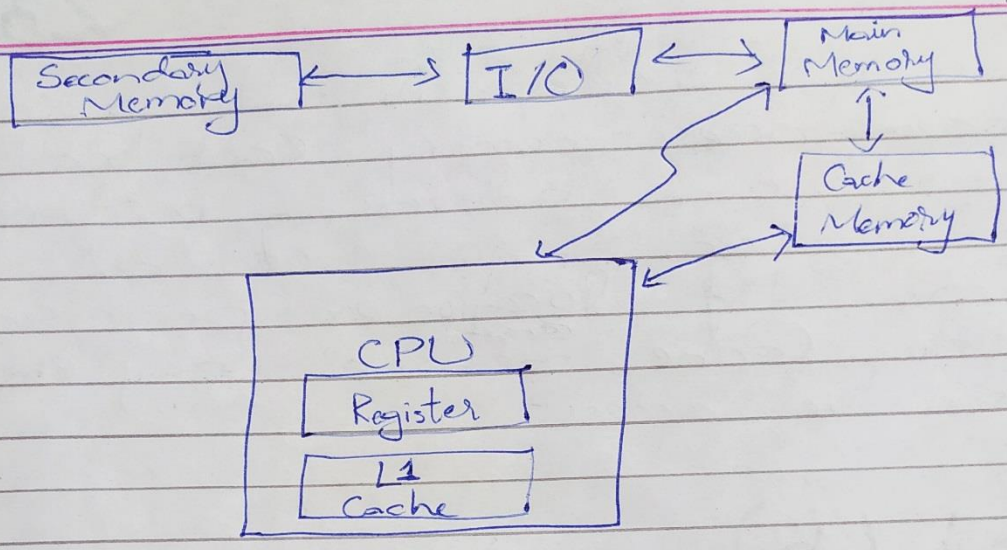
than its address. As with ordinary random-access memory, each location has its own addressing mechanism and retrieval time is constant independent of location or prior access patterns. Cache memories may employ associative access.

Part (b)

Principle of locality

Answer:-

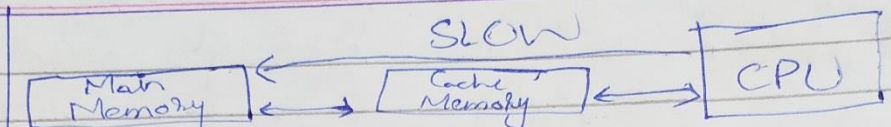
It refers to the tendency of the computer program to access information instructions whose addresses are near one another. The property of locality of reference is mainly shown by loops & subroutine calls in a program.

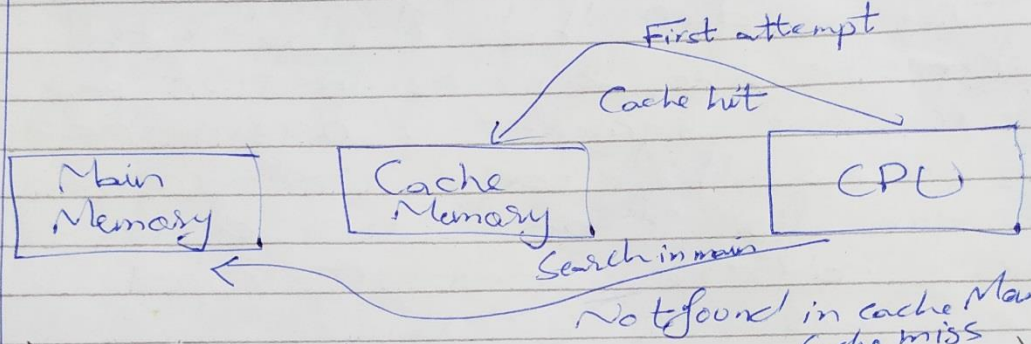


1.) In case of loop, in Program control processing unit repeatedly refers to the set of instructions that constitute the loop.

2.) In case of subroutine calls, every time the set of instructions are fetched from memory.

3.) References to data items also get localized that means same data item is referenced again & again.





In above figure, you can see that the CPU wants to read or fetch the data or instruction. First it will access the cache memory as it is near to it and provides very fast access. If the required data or instruction is found, it will be fetched. This situation is known as cache hit. But if the required data or instruction is not found in the cache memory then this situation is known as a cache miss. Now the main memory will be searched for the required data or instruction that was being searched

and if found will go through one of the two ways :-

1.) First way is that the CPU should fetch the required data or instruction & use it and that's it but what when the same data or instruction is required again.. CPU again has to access the same main memory location for it and we already know that the main memory is the slowest to access.

2.) The second way is to store the data or instruction in the cache memory so that if it is needed soon again in the near future it could be fetched in a much faster way.

Part: (c)

Possible approaches to Cache Coherency

Answer:-

Possible approaches to cache coherency include the following.

-) Bus Watching With Write Through:-

Each cache controller monitors the address lines to detect write operations to memory by other bus masters. If another master writes to a location in shared memory that also resides in the cache memory, the cache controller invalidates that cache entry. This strategy depends on the use of a write-through policy by all cache controllers.

-) Hardware Transparency :-

Additional hardware is used to ensure that all updates to main memory via cache are reflected in all caches. Thus, if one processor modifies a word in its cache, this update is written to main memory. In addition, any matching words in other caches are similarly updated.

→ Non-Cacheable Memory:-

Only a portion of main memory is shared by more-that one Processor, an this is designated as non-cacheable. In such a system all access to shared memory are cache misses, because the shared memory is never copied into the cache. The non cacheable memory can be identified using chip-select logic or high address bits.

Part:- (d)

Practical issues peculiar to SSDs

Answer:-

There are two practical issues peculiar to SSDs that are not faced by HDDs:-

→ SDD performance has a tendency to slow down as the device is used.
→ The entire block must be read

from the flash memory and placed in a RAM buffer.

→ Before the block can be written back to flash memory, the entire block of flash memory must be erased.

→ The entire block from the buffer is now written back to the flash memory.

→ Flash memory becomes unusable after a certain number of writes

→ Techniques for prolonging life.

→ Front ending the flash with a cache to delay and group write operations.

→ Using wear-leveling algorithms that evenly distribute writes across a block of cells.

→ Bad-block management techniques

→ Most flash devices estimate their own remaining lifetimes so system can anticipate & take preemptive action.

Part: (e)

Read CD write operation

Answer:-

READ:-

Information is retrieved from a CD or CD-ROM by a low-powered laser housed in an optical-disk player, or drive unit. The laser shines through the clear polycarbonate while a motor spins the disk past it. The intensity of the reflected light of the laser changes as it encounters a pit. Specifically, if the laser beam falls on a pit, which has a somewhat rough surface, the light scatters and a low intensity is reflected back to the source. The areas between pits are called lands. A land is smooth surface, which reflects back at higher intensity. The change between pits and lands is detected by a photo sensor and converted into a digital signal. The sensor tests the surface at regular intervals. The

beginning or end of a pit represent a 1; where no change in elevation occurs between intervals, a 0 is recorded.

NOTE:—

Recall that on magnetic disk, information is recorded in concentric tracks. With the simplest constant angular velocity (CAV) system, the number of bits per track is constant. An increase in density is achieved with multiple zoned recording, in which the surface is divided into a number of zones, farther from the centre containing more bits than zones closer to the centre. Although this technique increases capacity, it is still not optimal.

Question: 4 :-

Part : a :-

Solution :-

- The average time to access a word can be expressed as.

$(0.95)(0.01\,MS) + (0.05)(0.01\,MS + 0.1\,MS) =$
$0.0095 + 0.0055 = 0.015\,MS.$

- The average access time is much closer to 0.01 Ms than to 0.1 MS, as desired.

- Note : 95% at L1 cache and 5% at L2 cache

Part : C :-

Answer :-

Position	12	11	10	9	8	7	6	5	4	3	2	1
Bits	D8	D7	D6	D5	C8	D4	D3	D2	C4	D1	C2	C1
Block	1	0	1	0	-	1	0	1	-	0	-	-
codes	110	101	101	100	100	011	011	010	010	001	001	000
	0	1	0	1	0	1	0	1	0	1	0	1

The check bits are in bit numbers 8, 4, 2 and 1.
check bit 8 calculated by values in bit numbers:
12, 11, 10, and 9 (1010) = 0
check bit 4 calculated by values in bit numbers:
12, 7, 6, and 5 (1101) = 1.

check bit 2 calculated by values in bit numbers:
11, 10, 7, 6 and 3 (01100) = 0.
check bit 1 calculated by values in bit numbers:
11, 9, 7, 5 and 3 (00110) = 0.

Thus, the check bits are: 0010.

Part: D:-
Answer :-
Solution :-
Given data:-
Seek time = 6ms.
rotation speed = 7200.
number of sector = 500.
Size of each sector = 512b.

We have to read 2500 sector whic is approx 1.28 mb.
We know,
Disc access time = Avg. seek + Ag rotation latency + Transfer time.
7200 rotation require 60 sec.
1 rotation we can do in 8.4 ms.
∴ avg. rotation latency = 4.2 ms

Case: 1 :-
Data are ~~sto~~ store in continous way.
We need to read 5 track and in 1 rotation

We are reading 1 track
So to read 5 track
we need,
⇒ 5 x 6 ms = 30ms.
data is store in continous manner,
So the disc access time will be,

⇒ avg. seek time + Avg rotation latency for first time.
⇒ 6 + 4.2 + 30 ms.
⇒ 40.2 ms.

Case: 2 :-
Data store in random way.
As we know 1 track or 500 sector can be read in 8.4ms so, 2500 sector can read in, 42ms or 0.42 sec.
So, data is stored in Random way we have to deal with seek time
= 2500 x 8.4 ms = 20,5000 (ms)
or 20.5 (sec).

Similarly,
deal with rotation x latency = 2500 x 4.2
So, total disk access time
= 0.42 + 20.5 + 10.5
= 31.42 sec.

Part : B :-

Answer :-

Tag (9) / Set (13) / word (2) 177H / 0FEEH / 3H