Truth table.

A	B	Q_0	Q_1	Q_2	Q_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Q1 (part C)

Decimal to BCD encoder.

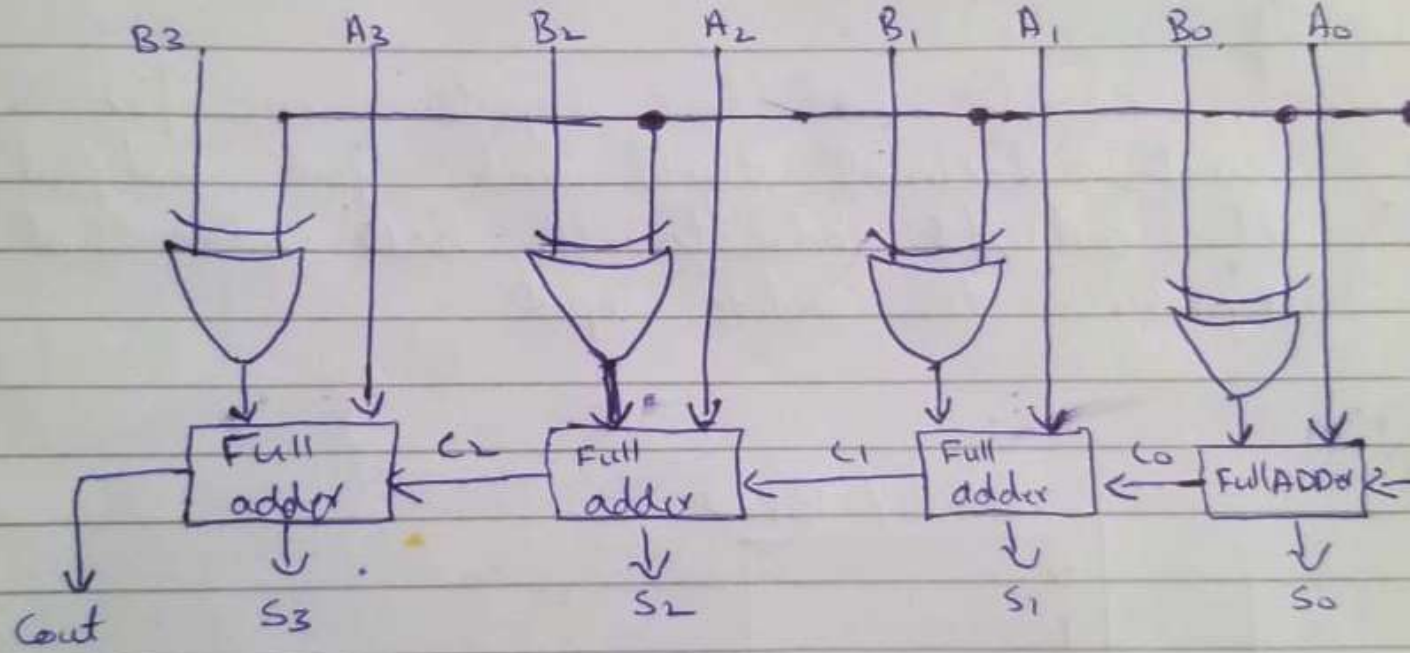
Sol:

encoder has ten inputs - one for each decimal digit and four outputs the outputs indicate the BCD code that represend the active input.

(Q1) Draw and explain the logic diagram

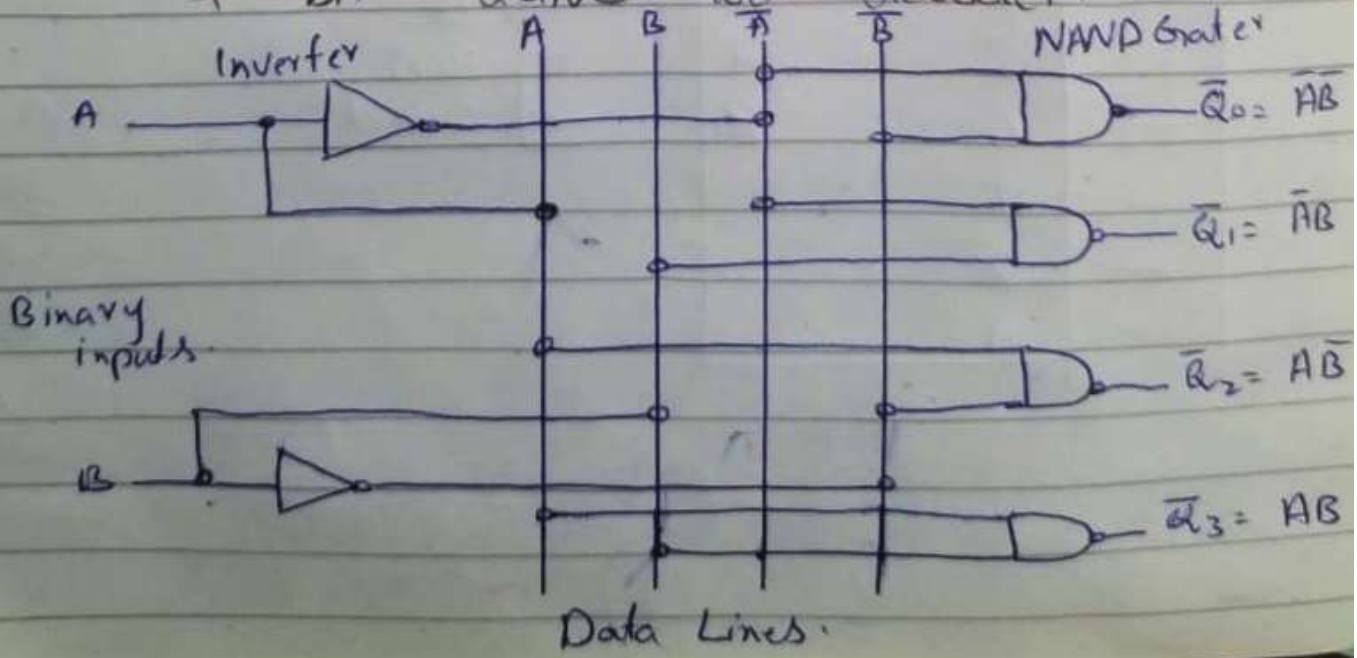
(a) A Circuit for adding or Subtracting two 4-bit numbers.

Ans In Digital Circuit, A binary Adder-Subtractor is one which is capable of both addition and subtraction of binary numbers is one Circuit itself. it is one of the Components of (ALU)



Q(1)(b)

4 bit active low decoder.



Q2

Example 2: 4x1 mux

A 4x1 mux has 4 input lines (D_0, D_1, D_2, D_3) two select input (S_0 & S_1). and one output line Y. (see Figure 3)

if $S_1S_0 = 00$. then $Y = D_0$

IF $S_1S = 01$. then $Y = D_1$

IF $S_1S_0 = 10$. then $Y = D_2$

IF $S_1S_0 = 11$. then $Y = D_3$

Thus the output signal Y can be expressed as:

$$Y = \underbrace{S_1S_0}_{\text{minterm } m_0} D_0 + \underbrace{S_1S}_{\text{minterm } m_1} \circ D_1 + \underbrace{S_1\bar{S}_0}_{\text{minterm } m_2} D_2 + \underbrace{S_1S_0}_{\text{minter } m_3} D_3$$

obviously, the input selected to be passed to the output depends on the minterm expression of the select inputs.

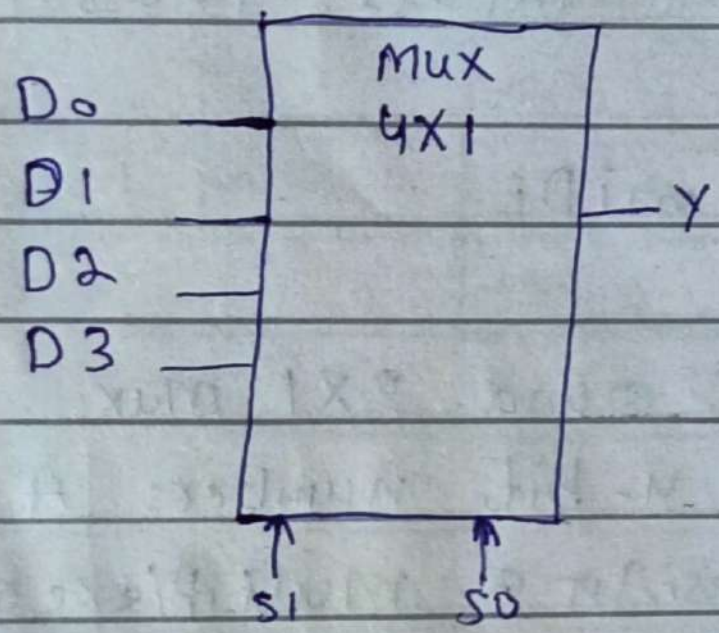


Figure 3: A 4x1 Multiplexer

in General:

For MUXes with n select inputs, the output Y is

Given by

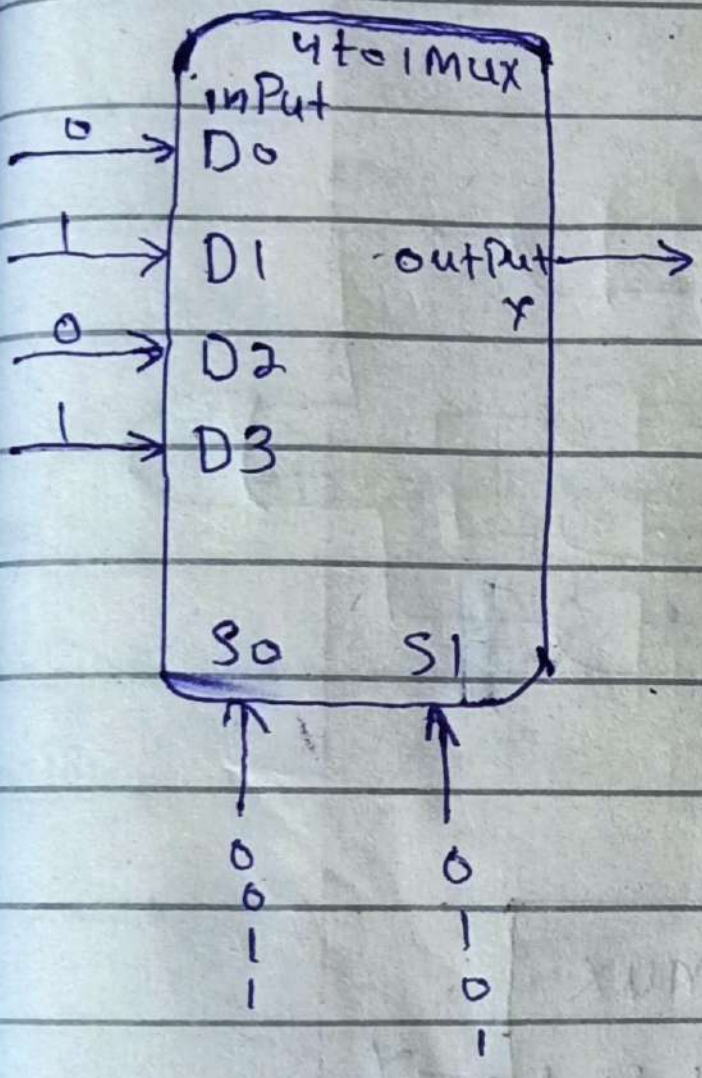
$Y = m_0 D_0 + m_1 D_1 + m_2 D_2 + \ldots\ldots + m_{2^n-1} D_{2^n-1}$

where m_i = i^{th} minterm of the select inputs Thus.

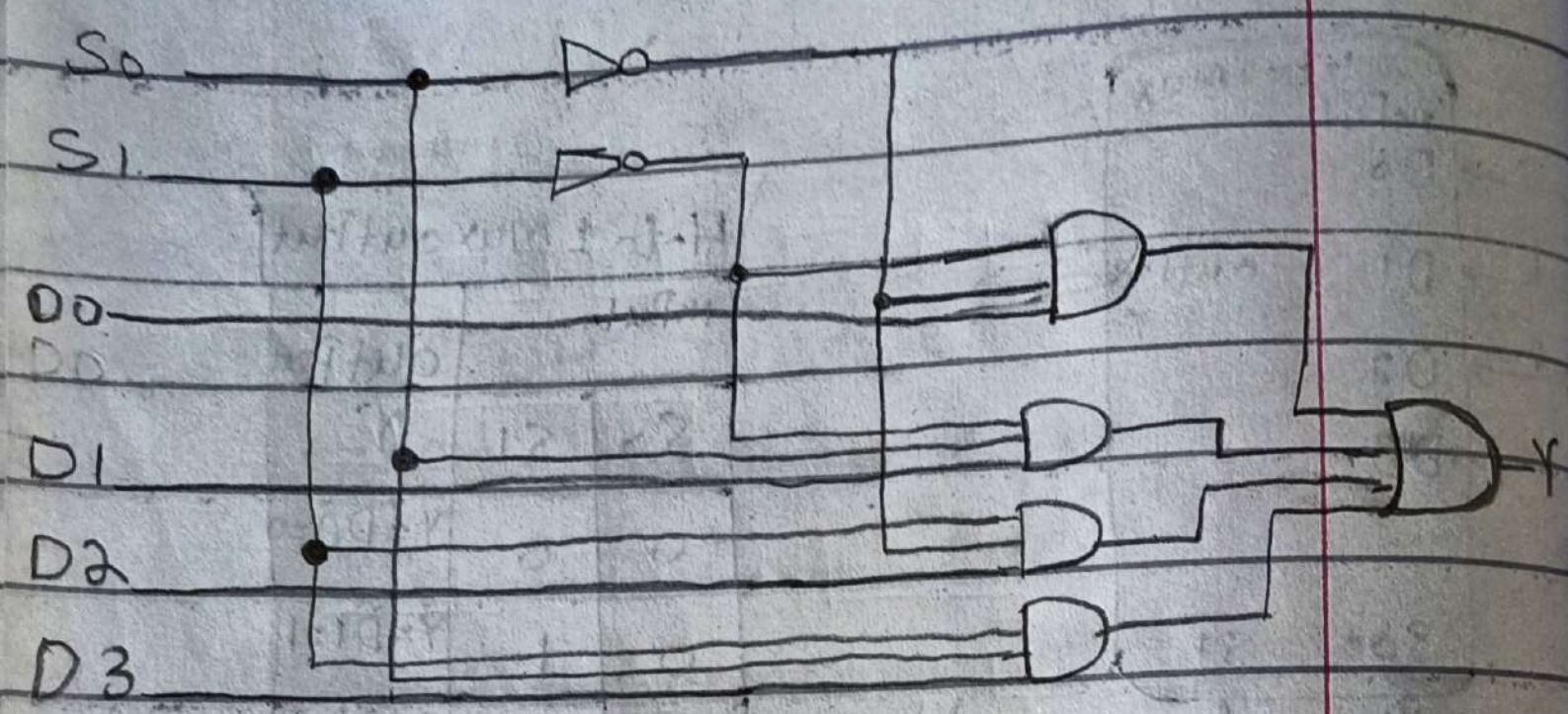
$$Y = \sum_{i=0}^{2^x-1} m_i D_i$$

Example 3: Quad 2X1 Mux

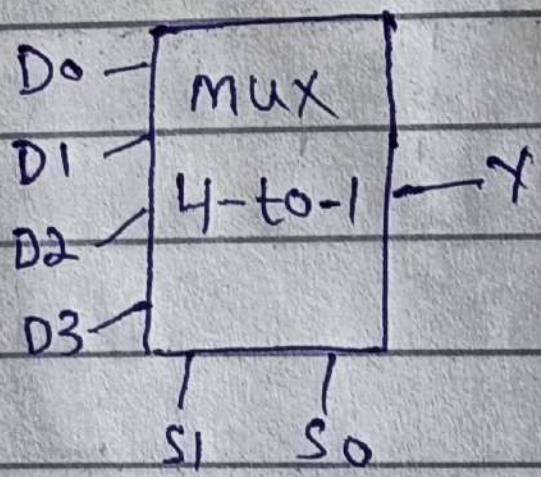
Given two 4-bit numbers A and B, design a multiplexer that select one of those 2 numbers based on some select signal S. obviously. the output (Y) is a 4-bit number.



4-to 1 Mux outPut		
inPut		outPut
S0	S1	Y
0	0	Y=D0=0
0	1	Y=D1=1
1	0	Y=D2=0
1	1	Y=D3=1

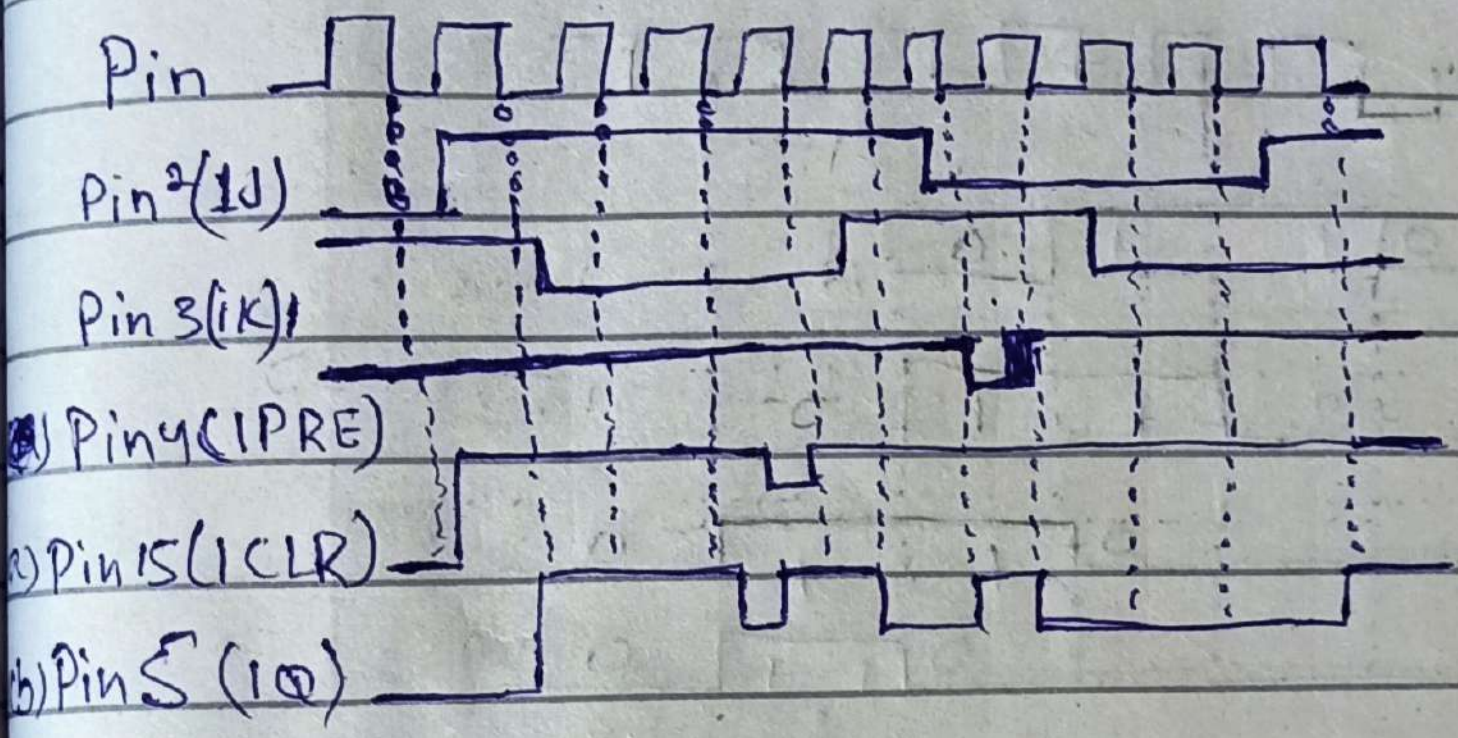


S1	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

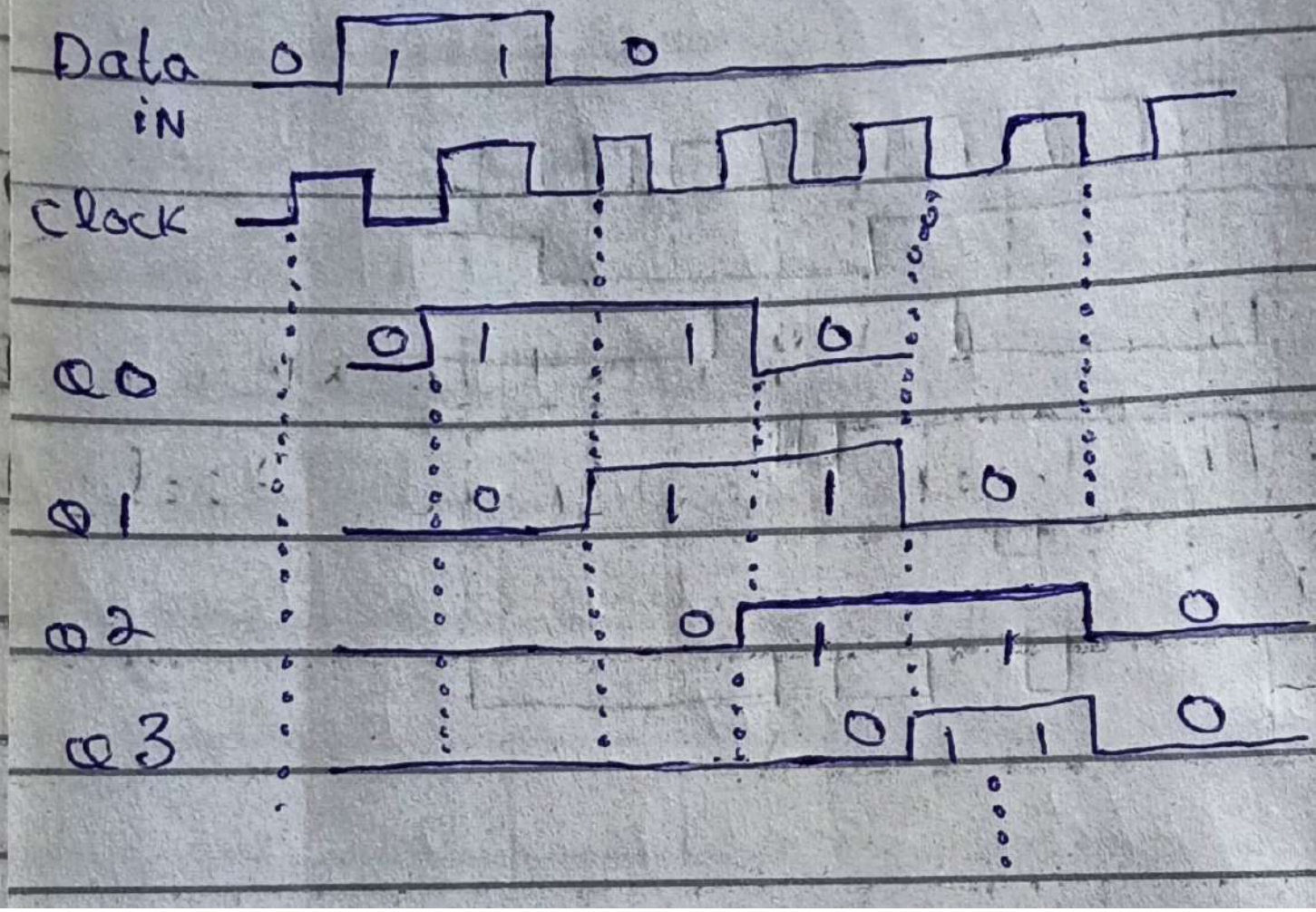


Determine the Boolean expression for Y as a function of Di and Si.

@4



(Q5)

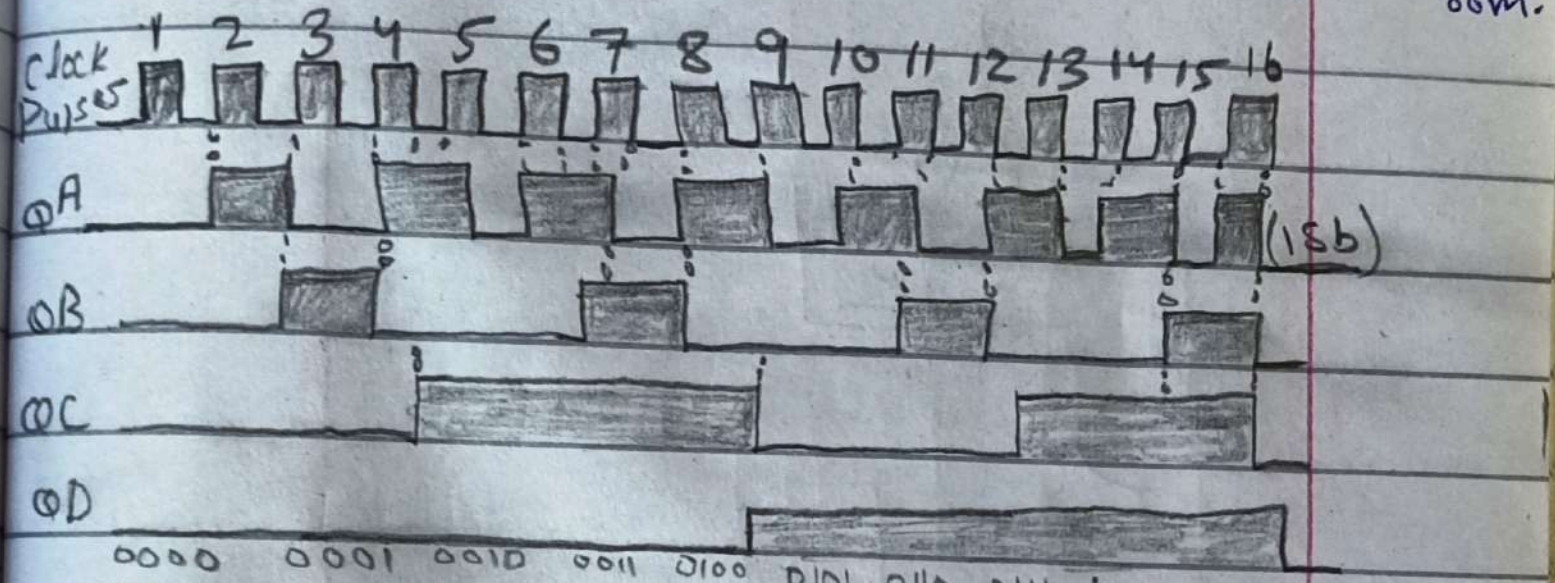


Synchronous Counters.
are different from ripple counters in that clock pulses are applied to the inputs of all flip-flops. A common clock triggers all flip-flops simultaneously rather than one at a time in succession as in a ripple counter.

Binary Counter:

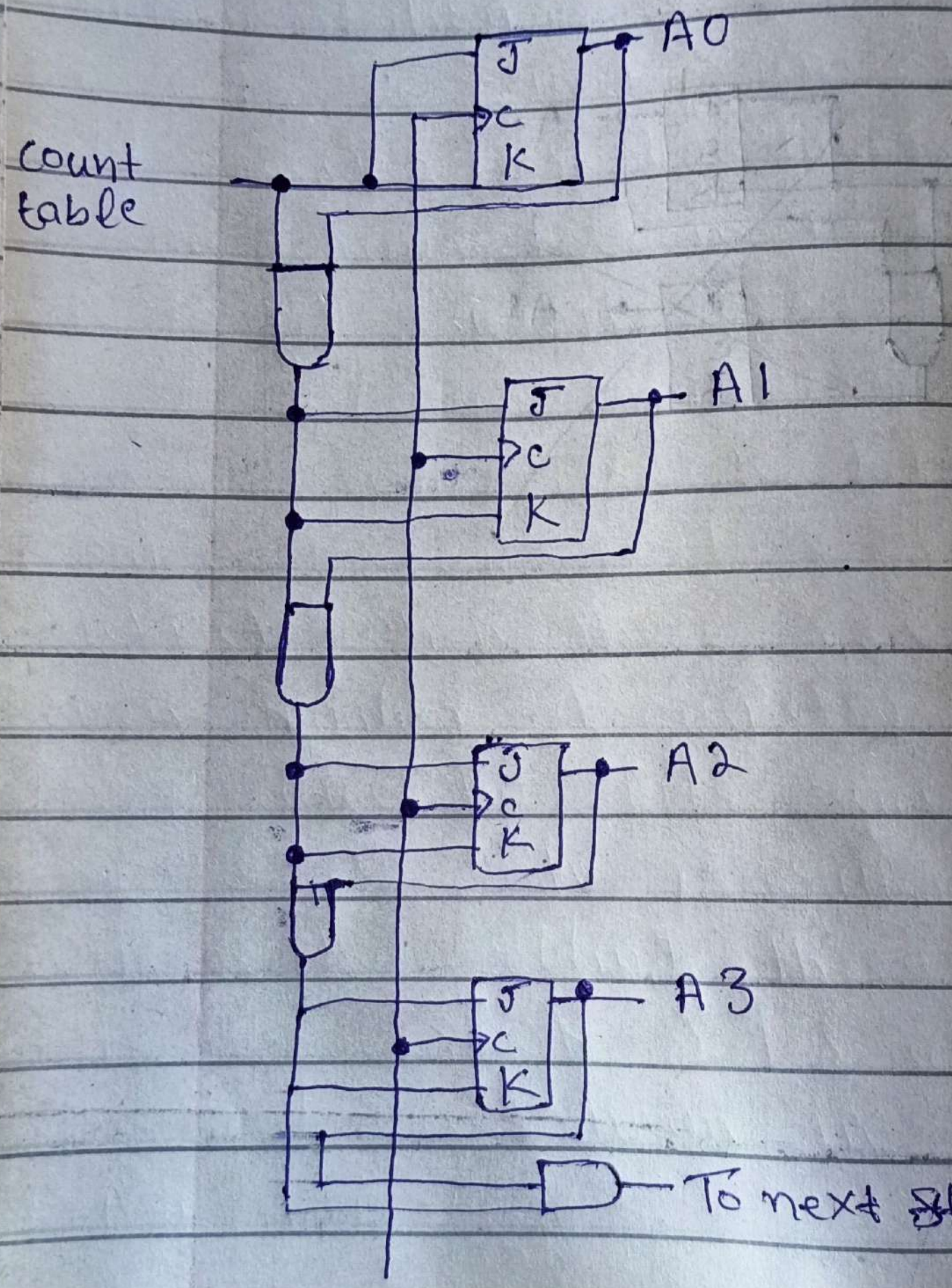
The design of a synchronous binary counter is so simple that is no need to go through a sequential logic design process.

Q6) Synchronous counter waveform Timing Diagram.



1100 1101 1110 1111 0000

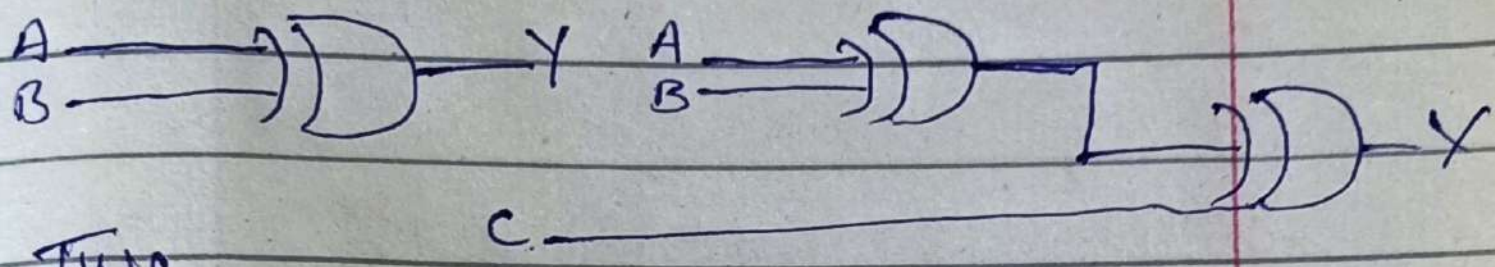
13 13 14 15 0


count
table
J
C
K
A0
J
C
K
A1
J
C
K
A2
J
C
K
A3
To next stage.

Q3

Parity generators and checker. logic circuit that generates the Parity bit in the transmitter. on the other hand, a circuit that checks the Parity in the receiver is called Parity checker. A combined circuit or divices of Parity generators and Parity cheakers are commonly used in digital system to detect the single bit erros in the transmitted data word. The basic Principle involved in the

implementation of Parity Circuits is that sum of odd number of 1s always 1 and sum of even number of 1s is always zero. such error detecing and correction can be using EX-OR gates (since EX-OR Produce zero outPut when there are even number of inPuts.)
To Produce two bits sum one EX OR gate is suffcient wheses for adding three bits two EX-OR gates are required as shown in below fidure



Two Bits

Three Bits