ASSIGNMENT # 5

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Subject : Computer Architecture

Submitted : Sir Amin

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Question # 1

(a) Discuss different types of semiconductor memories in detail?

(Ans) **Types Of Semiconductor Memories**

There are various types of semiconductor memories. The most common is reffered to as RAM (Random Access Memory) Most types have the property of Random Access Memory which means that it take the same amout of time to access any memory location. Here is a table of semiconductor Memory types.

Memory Type	Category	Erasure	Unit Mechanism	Volatility
RAM (random memory)	Read / write memory	Electrically Bite level	Electrically	Volatile
ROM	Read only memory	Not possible	Masks	Non Volatile
PROM	//	//	//	//
EPROM	//	UV-light chip level	//	//
EEPROM	//	electrically byte level	//	//
Flash memory	Read mostly memory	Electrically block level	Electrically	//

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(c)

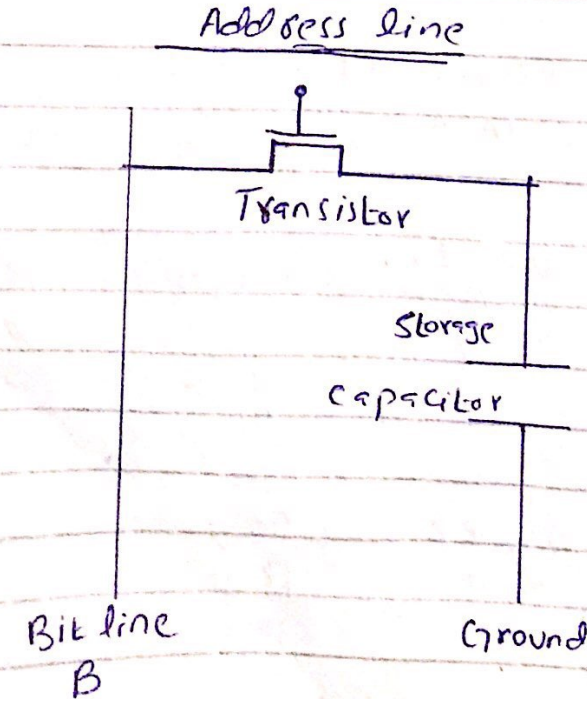
(a) Explain the read and write operation for the ~~SRAM~~ DRAM ?

Ans) READ OPERATION :

When the address line is selected the transistor turns on and the charge stored on the capacitor is fed out onto a bit line and to a sense amplifier. It compares the capacitor voltage to a refrence value and determines if the cells contains a logic 1 or a logic 0.

WRITE OPERATION :

A voltage signal is applied to a bit line a high voltage represents 1 & a low represents 0.



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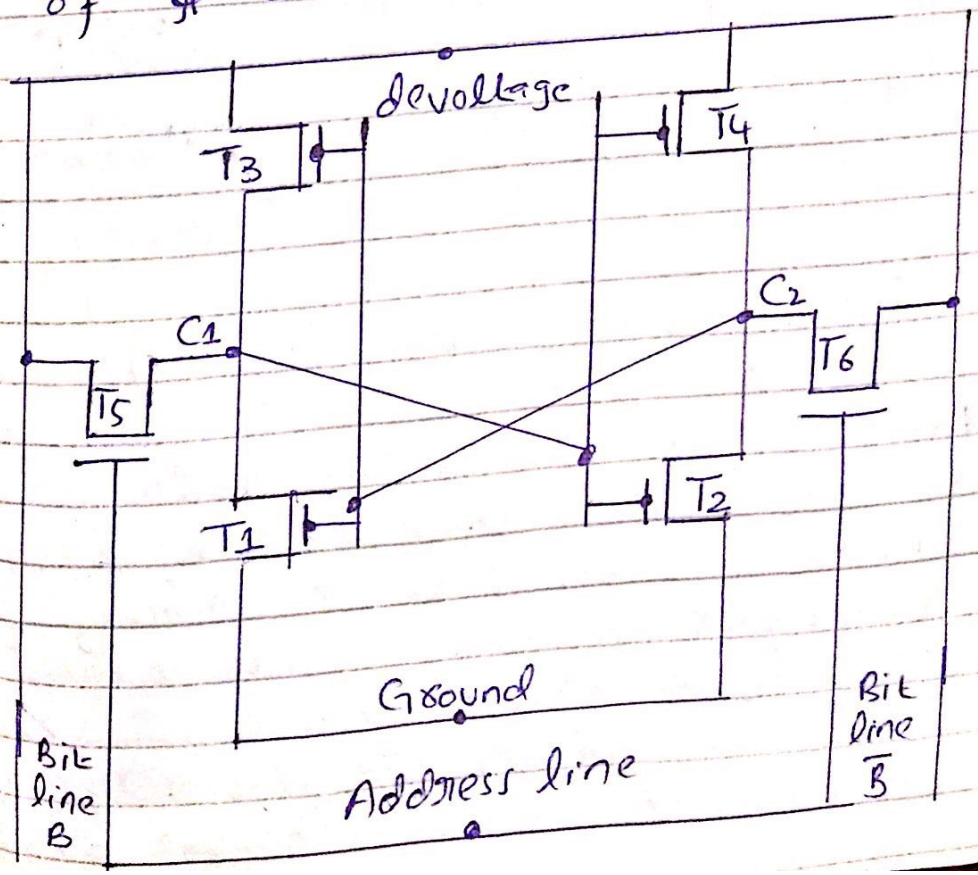
(b) Explain the read and write operation for the SRAM cell using diagram ?

Ans) READ OPERATION :

In SRAM, for any operation to be performed, the word line should be high. To perform read operation initially, A voltage signal is applied to the list line high voltage 1, low voltage 0.

WRITE OPERATION :

Consider the memory bits consists of $\phi = 0$ and $\phi' = 1$



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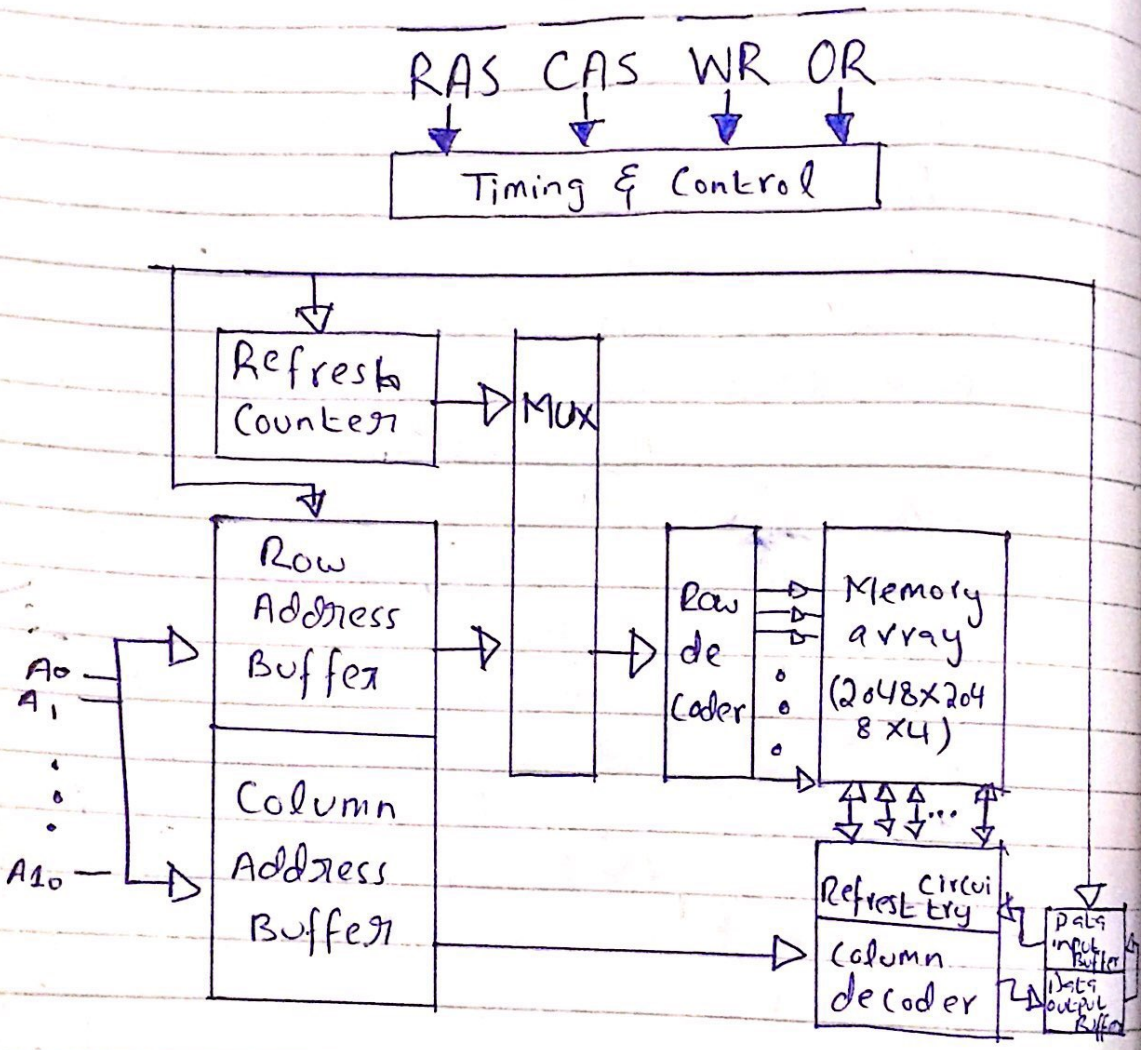
(d) Discuss 16-Mbit DRAM (4M x4) organization using diagram ?



Typical 16-Mbit DRAM (4M x4)

Because only 4 bits are read/written to this DRAM, there must be multiple DRAMs connected to the memory controller to read/write a word of data to the bus.

All the DRAMs require a refresh operation. A simple technique for

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refreshing is, in effect, to disable the DRAM chip, while all data cells are refreshed. The refresh counter steps through all of the row values. This causes each cell is row to be refreshed.

(e) Discuss 1MB (256K x 4 x 8 Bit) memory organization using diagram.

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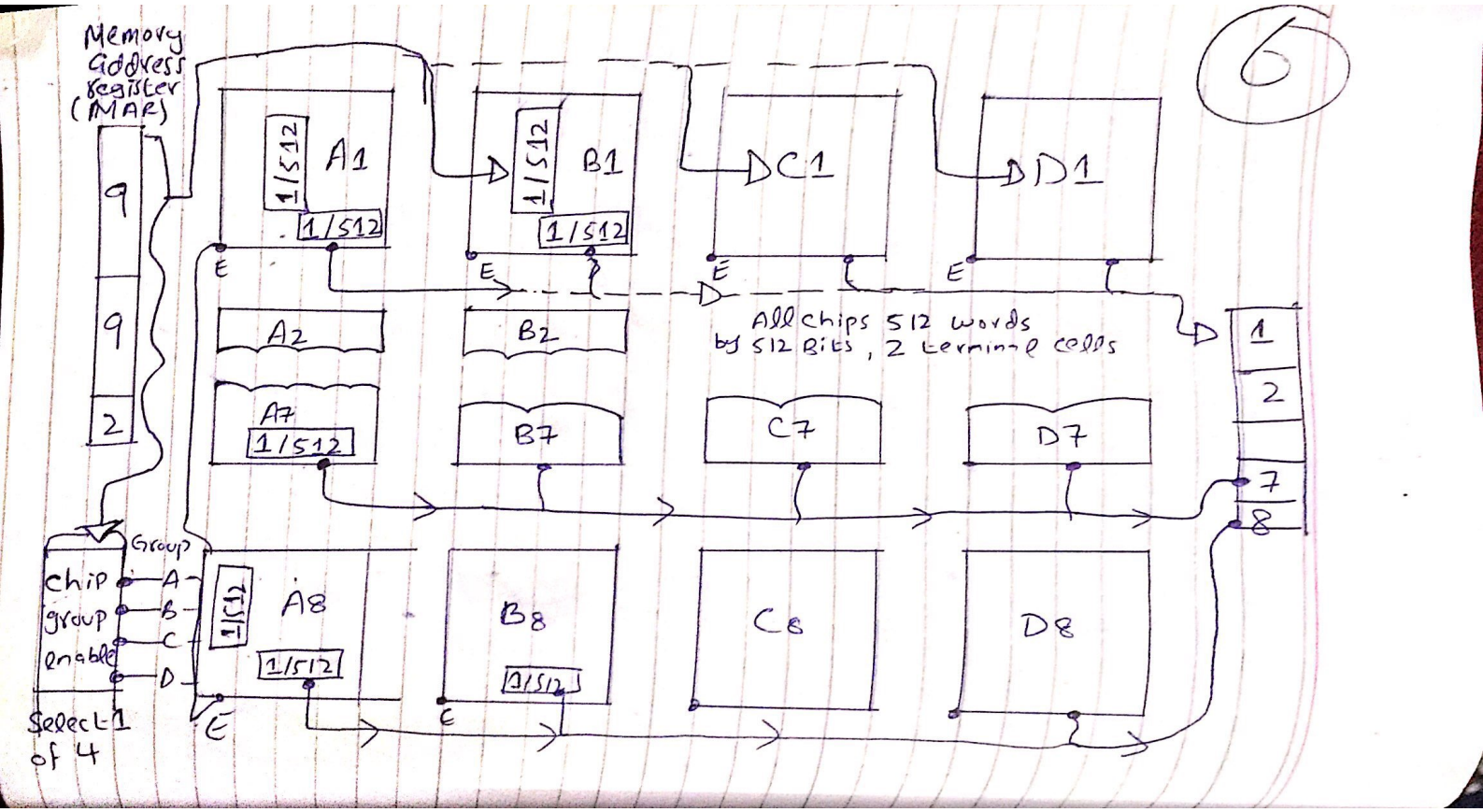

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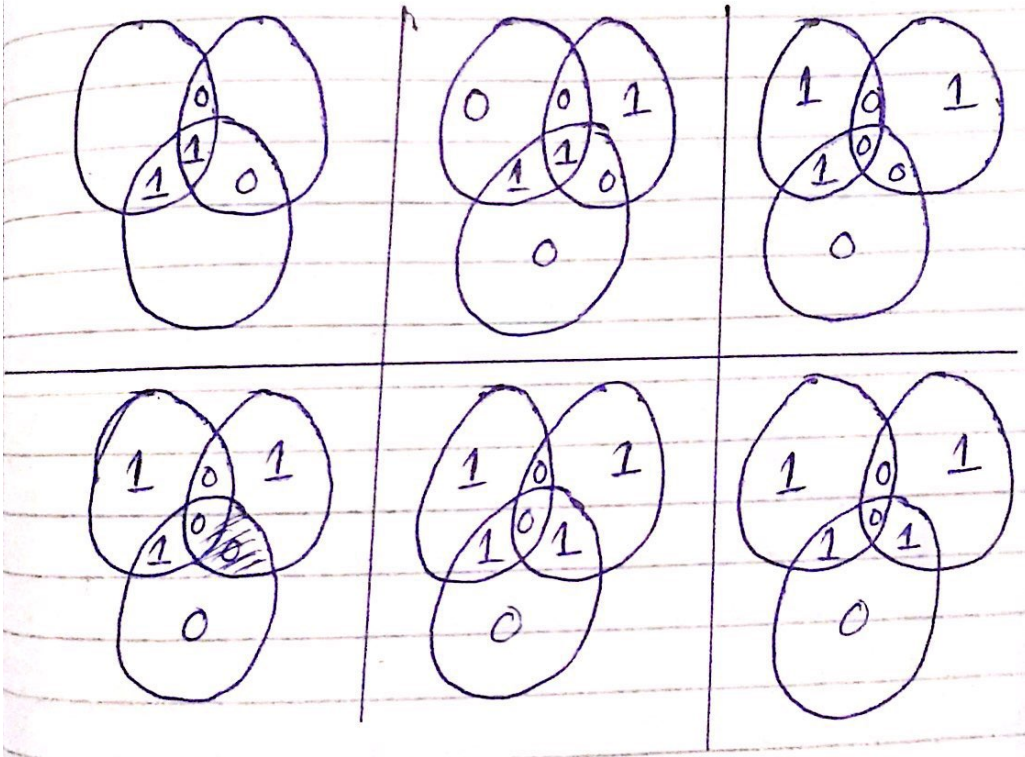
The possible organization of a memory consisting of 1M word by 8 bits per word. In this case we have four columns of chips, each column containing 256K words arranged.

(f) Explain Hamming SEC-DEC code using venn diagram?



Hamming SEC-DEC Code

With 1 bit-per chip organization an SEC-DEC code is generally considered adequate. e.g the IBM 30xx implementations used on 8-bit SEC-DEC code for each 64 bits

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of data in main memory. The size of main memory is actually about 12%. larger than is apparent to the user. The VAX Computer used a 7-bit SEC-DED for each 32 bits of memory, for a 22%. overhead.

(g) How is syndrome for the Hamming Code interpreted?

Ans) Syndrome for the Hamming Code interpreted as follows.

* If the syndrome contains all 0s, no error has been detected.
* If Syndrome contains one and only one bit set to 1, then an error has occured in one of the 4 check. No Correction is needed.
* If the syndrome contains more than one bit set to 1, then the numerical value of the syndrome indicates the position of the data bit in error. This data bit is invested for correction.

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Question # 2

(a) DRAM & SRAM ?

DRAM :

- DRAM is more ~~done~~ dense and less expensive.
- DRAM requires the supporting refresh circuitry.
- DRAM are normal in speed.
- DRAM is used for main memory.

SRAM :

- SRAM is expensive.
- SRAM does not require any refresh circuitry.
- SRAM are ~~fa~~ faster in speed than DRAM.
- SRAM is used for Cache memory.

(b) EEPROM & flesh memory ?

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EEPROM :

- EEPROM devices can erase any byte of memory at any time.
- EEPROM uses NOR type memory.
- EEPROM is byte-wise erasable.

FLASH MEMORY :

- Flash memory can only erase an entire chunk, or "sector" of memory at a time.
- Flash memory uses NAND type memory.
- Flash is block-wise erasable.

C) Hard failure & Soft error in semiconductor memories?

Ans) A hard failure is a permanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically b/w 0 & 1. Hard errors can be caused by harsh environment abuses, manufacturing defects, and wear.

Where as

Soft error is a random, nondestructive even that alters the contents of

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one or more memory cells without damaging the memory. Soft errors can be caused by power supply problems or alpha particles.

Question # 3

Solution:

Position	12	11	10	9	8	7	6	5	4	3	2	1
Bits	D8	D7	D6	D5	D4	D3	D2	D1	C4	C3	C2	C1
Block	1	0	1	0	-	1	0	1	-	0	-	-
Codes	1100	1011	1010	1001	1000	0111	0110					

Position	12	11	10	9	8	7	6	5

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Question # 3

Position	12	11	10	9	8	7	6	5	4	3	2	1
Bits	D8	D7	D6	D5	C8	D4	D3	D2	C4	D1	C2	C1
Block	1	0	1	0	–	1	0	1	–	0	–	–
Codes	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001

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The check bit one in bit numbers 8, 4, 2 and 1 Check bit 8 calculated by values in bit numbers 12, 11, 10 and 9 = 0
check bit 4 Calculated by values in bit 12, 7, 6 & 5 = 1
check bit 2 Calculated by values in 11, 10, 7, 6 & 3 = 0
check bit 1 Calculated by values in 11, 10, 9, 7, 5 and 3 = 0
Thus the check bit give = 0010

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