

Name	-	M-Usama
ID	-	14150
Subject	-	Micro-Processor
Submitted To	-	Engr. Aamir Ameen
Date	-	24/09/2020.

(1)

Q-1

Part # A

Explain The Process of sequential & priority handling of interrupts.

① Sequential handling Interrupts:-

An Interrupt is a signal from a device which cause a main program which is operating a computer to stop & figure out what it must do next.

- The sequential multiplexed interrupts work by handling the interrupts in a strict sequential order.

② Priority handling in interrupts:-

A priority interrupt is a system which decides the priority at which various devices, which generates the interrupt signal at the same time, will be serviced by the CPU when two or more device interrupts the computer simultaneously. The computer services the device with the higher priority first.

(2)

Q: 2

Part B

Explain interrupt Vector Table (IVT).

Ans It is a table in the lowest 1KB of memory which contains pointers to ISRs.

- The type code received from PIC on data bus is multiplied by 4, to get the physical address from where it search from the pointer of ISR in the table for the device which had sent the interrupts request to CPU.

Interrupt Type code	Description	Pointer addressing	Points to
00	Divide By zero	00000	7845:00CE
04	over flow	00010	0070:0756
05	Pointer to screen	00014	F000:FF54
08	Clock Tick	00020	93E2:0174
09	Keyboard action	00024	2C3A:14BA
0B	COM2	0002C	F000:210D
0C	COM1	00030	F000:210D
0E	Floppy Disk 1	00038	2106:0439
0F	LPTT Pointer	0003C	0070:0756
19	Bootstrap startup Routine	00064	0070:18ED

(3)

Q-2

Part A

Here Two Techniques To solve The Problem of Twice keys are depressed in same Time.

• In old generation computers, When we depress The Two or more keys at same Time So The computer donot work.

No one Key will be Taken or selected. Both keys are lockout.

• New generation computers,

When Two or more

Keys are selected at same Time so

• The first released or free key is selected of The both keys. and The second depress then The first one is second selected by The computer.

• First release is select first.

• second release key is selected 2nd.

(4)

Q-2

Part # B

Rate generator ~~and~~ operation.

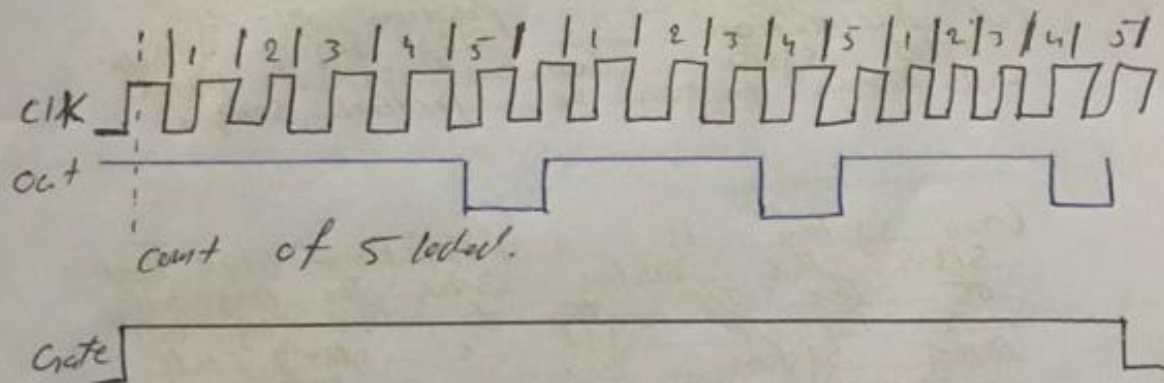
(Initial value $N=5$)

It divides in input clock frequency by N .

When the counting starts, o/p becomes high.

after 4 pulses, the output goes low for 1 clock period so for N clock cycles.

1 output cycle is generated. Gate must remain high during counting.



(5)

Q-3

Part # A

(DMA Process)

- ① The device sends DMAC request for data transfer.
- ② The DMAC sends high on HOLD input of CPU.
- ③ The CPU programs the DMA controller.
 - I/O Device address.
 - starting address of main memory block for data.
 - Amount of data to be transferred.
- ④ CPU sends HLDA to DMAC & releases the control of system bus.
- ⑤ DMA controller sends ACK to the device which sent its request initially.
- ⑥ DMA deals with transfer.
- ⑦ When done, the device sends low on DREQ pin to DMAC.
- ⑧ The DMAC sends low on HOLD pin, telling CPU to acquire the control of system bus.

(6)

Q-3

Part B Diff b/w Asynchronous & Synchronous
Serial Communication -

Ans The protocols for serial data transfer
can be grouped into two types. Synchronous
& Asynchronous.

For synchronous data transfer, both the
sender & receiver access the data
according to the same clock -

For asynchronous data transfer, there
is no common clock signal between
the sender & receiver.

(7)

Q-4

Part # A

(Status signal)

~~When it is high (1) The address on the address bus is for input-output or memory.~~ which determines the whether

When it is high (1) The address on the address bus is for input-output devices.

When it is low (0) The address on the address bus is for the memory.

S₀, S₁ - These are status signals.

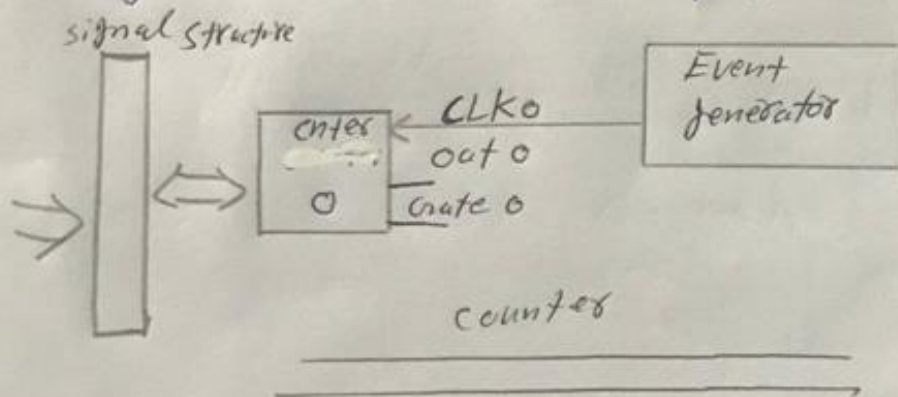
Q=5

Part # A

82C54 as a counter:-

It counts the events.

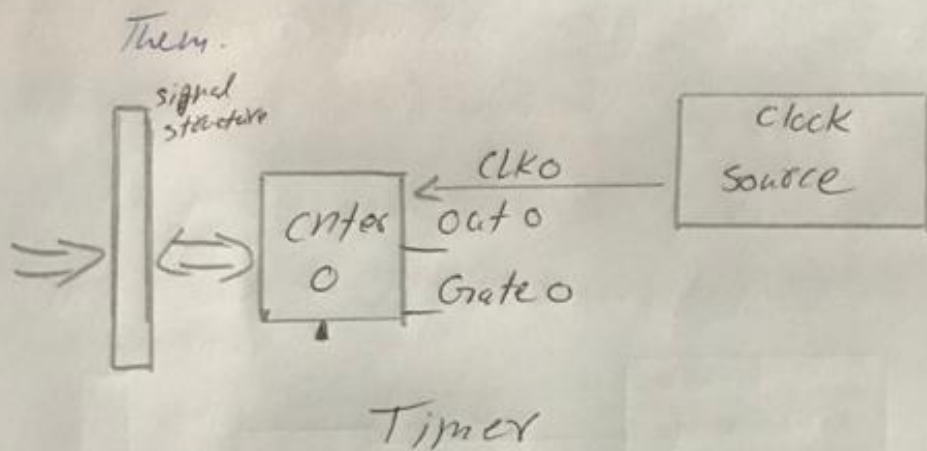
The pulses generated by the occurrence of event are connected at its CLK input & the counter counts them. The events may be periodic or A-periodic.

For Timer

It is used to produce delay between two events.

P-T-O

The pulses generated by the periodic clock source are connected at its CLK input of the timer counts



Q = 5

Port # 13

RS 432 interface

Ans RS-432 is simple universal, well understood and supported but it has some serious shortcomings as a data interface - The standard is to 256 KBPS or less & line lengths of 15 M (50 ft) or less but today we see high speed sports on our home PC running very

High speeds and with high quality cable maximum distance has increased greatly - The rule of Thumb for the length a data cable depends on speed of the data, quality of the cable.

