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Subject : Computer Architecture

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Muhammad Musa, Computer Architecture

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Q1:

Ans:(A) 1. Data Processing:-
Data may take a wide variety of forms, and the range of processing requirements is broad.

2. Data Storage:-
The computer performs a long-term data storage function.

3. Data Movement:-
When data are moved over longer distances, to or form a remote device, the process is known as "data communication".

4. Control:-
Within the computer, a control unit manages the computer's resources and orchestrates the performance of its functional parts in response to instructions.

ns:(B) • ISU:(instruction Sequence unit):
Determines the sequence in which instructions are executed in what is referred to as a superscalar architecture.

- IFU (instruction fetch unit):- Logic for fetching instructions.
- IDU (instruction decode unit):- The IDU is fed from the IFU buffers, and is responsible for the parsing and decoding of all z/Architecture operation codes.
- LSU (Load-store unit):- It is responsible for handling all types of operand acesses of all lengths, modes, and formats as defined in z/Architecture.
- XU (translation unit):- This unit translates logical addresses from instructions into physical addresses in main memory.
- FXU (Fixed-point unit):- The FXU executes fixed-point arithmetic operations.
- BFU (binary floating-point unit):- The BFU handles all binary and hexadecimal floating-point operations.
- DFU (decimal floating-point unit):- The DFU handles both fixed-point and floating-point operations on numbers that are stored as decimal digits.
- RU (recovery unit): The RU keeps a copy of the complete state of the

system that includes all registers, collects hardware fault signals.

- COP (dedicated co-processor):- The COP is responsible for data compression and encryption functions for each core.
- I-cache:- This is a 64-KB L1 instruction cache, allowing the IFU to prefetch instructions before they are needed.
- L2 control:- This is the control logic that manages the traffic through the two L2 caches.
- Data L2:- A 1-MB L2 data cache for all memory traffic other than instructions.
- Instr-L2:- A 1-MB L2 instruction cache.

Ans:(C) The IAs operates by respectively performing an instruction cycle. Each instruction cycle consists of two-sub-cycles.

(a) Fetch Cycle:- The opcode of next instruction is loaded into the IR and the address portion is loaded into the MAR. The instruction may be taken from the IBR, or it can be obtained from memory by loading a word into the MBR, and then down to the IBR, IR and MAR.

(b) Execute Cycle:- The control circuitry interprets the Opcode and executes the instruction by sending out the appropriate control signals to cause data to be moved or an operation to be performed by the ALU.

Ans:(D) a. No, These programs are never considered to be embedded because they are not an integral component of a larger system.

b. Yes, regardless of what the disk drive is used for. The Software within the disk drive controls the HDA (Hard disk assembly) hardware and is hard real time as well.

c. No, Input-Output drivers do not represent the embedded system.

d. Yes, PDA is an embedded system because it is just like a personal computer in hand.

e. Yes, the firmware in the cell-phone is controlling the radio hardware.

f. Yes, these computers are considered an embedded system because the software running in those computers control the radar hardware; therefore, the computers are an integral component of a large system.

g. If the FMS is not connected to the avionics and is used only for logistics computerizations, a function readily performed on a laptop, then the FMS is clearly not embedded.

h. Yes, both in the simulator, and in the thing being tested in the HIL simulator. Hardware is being controlled on both sides.

i. Yes, in this case of the "system" is the combination of the pacemaker and the person's heart.

j. Yes, it is part of a large system, the engine, and it is directly monitoring and controlling the engine through special hardware.

Q2:-

Ans:(A) There are four main structural components:

1. Central Processing Unit (CPU):- It controls the operation of the computer and perform

its data processing functions; often simply referred to as processor.

2. Main memory:-
It stores data.

3. I/O:-
It moves data between the computer and its external environment.

4. System interconnection:-
Some mechanism that provides for communication among CPU, main memory and I/O.

Ans:(B) The characteristics of a family are as follows:

- Similar or identical instruction set:-
In some cases, the lower end of the family has an instruction set that is a subset of that of the top end of the family.
- Similar or identical operating system:-
The same basic operating system is available for all family members.
- Increasing Speed:-
The rate of instruction execution increases in going from lower to higher family members.
- Increasing number of I/O ports:-
The number of I/O ports increases in going from lower to higher family members.
- Increasing memory size:-
The size of main

memory increasing in going from lower to higher family members.

- Increasing cost:-
  At a given point in time, the cost of a system increases in going from lower to higher family members.

Ans:(C) Stored-program Computer:-
"A fundamental design approach first implemented in the IAS computer is known as stored-program computer."
This idea is usually attributed to the mathematician John von Neumann. In 1946, von Neumann and his colleagues began the design of a new stored-program computer, referred to as the IAS computer, at the Princeton institute for Advance Studies.
It consists of:

- A main memory, which stores both data and instructions.
- An arithmetic and logic unit (ALU) capable of operating on binary data.

Ans:(D) Moore's Law:-
It was propounded by Gordon Moore, cofounder of Intel in 1965.

Moore observed that the number of transistors that could be put on a single chip was doubling every year.
The consequences of Moore's Law are profound:

1. The cost of computer logic and memory circuitry has fallen at a dramatic rate.
2. Because logic and memory elements are placed closer together on more densely packed chips, the electrical path length is shortened, increasing operating speed.
3. The computer becomes smaller, making it more convenient to place in a variety of environments.
4. There is a reduction in power requirements.
5. With more circuitry on each chip, there are fewer interchip connections.

Q3.-

Ans.(A) Computer Architecture:-
It refers to those attributes of a system visible to a programmer, or put another way, those attributes that have a direct impact on the logical execution of a program.
A term that is often used interchangeably with computer architecture is

instruction set architecture (ISA).

Computer Organization:- It refers to the operational units and their inter-connections that realize the architectural specifications. Examples of architectural attributes include the instruction set, the number of bits used to represent various data types (e.g numbers, characters), I/O mechanisms, and techniques for addressing memory.

Ans:(B) CISC:- The current x86 offerings represent the results of decades of design effort on complex instruction set computers (CISCs). The x86 incorporates the sophisticated design principles once found only on mainframes and supercomputers and serves as an excellent example of CISC design.

RISC:- An alternative approach to processor design is the reduced instruction set computer (RISC). The ARM architecture is used in a wide variety of embedded systems and is one of the most powerful and best-designed RISC-based systems on the market. In this section and the next. we provide a brief overview of these two systems.

Ans:(C) **Microprocessor:-**

Microprocessor chips include registers, an ALU, and some sort of control unit or instruction processing logic. As transistor density increased, it became possible to increase the complexity of the instruction set architecture, and ultimately to add memory and more than one processor.

Microcontroller:-

A microcontroller is a single chip that contains the processor, non-volatile memory for the program (ROM), volatile memory for input and output (RAM), a clock, and an I/O control unit. The processor portion of the microcontroller has a much lower silicon area than other microprocessor and much higher energy efficiency.

Ans:(D) **Cortex-A:-**

The cortex-A and cortex-A50 are application processors, intended for mobile devices such as smartphones and eBook readers, as well as consumer devices such as digital TV and home gateways (e.g DSL and cable internet modems). These processors run at higher clock frequency (over 1GHz), and support a memory management unit (MMU).

Cortex-R:-
The cortex-R is designed to support real-time applications, in which the timing of events needs to be controlled with rapid response to events. They can run at a fairly high clock frequency and have very low response latency.

Cortex-M:-
Cortex-M series processors have been developed primarily for the microcontroller domain where the need for fast, highly deterministic interrupt management is coupled with the desire for extremely low gate count and lowest possible power consumption.

Q4:-
Ans (A) 1. LH instruction = 010FA
opcode = 01 , address = 0FA

RH instruction = 210FB
opcode = 21 , address = OFB

Now convert numbers to binary form:
LH instruction:
01 = 00000001 = LOAD M(X)
= LOAD M(OFA)
RH instruction:
21 = 00100001 = STOR M(X)
= STOR M(OFB)
Hence the assembly language code for 08A 010FA210FB is
LOAD M(OFA)
STOR M(OFB)

2. LH instruction = 010FA
opcode = 01 , address = OFA

01 = 00000001 = LOAD M(X)
= LOAD M(OFA)
RH instruction = OF08D
opcode = OF , address = 08D

OF = 00001111 = JUMP + M(X, 0:19)
= JUMP + M(08D, 0:19)
Hence the assembly language for 08B 010FAOF08D is

LOAD M(OFA)

JUMP + M(08D, 0:19)

3. LH instruction = 020FA
opcode = 02 , address = OFA

02 = 0000010 = LOAD - M(X)
= LOAD - M(OFA)

RH instruction = 210FB
opcode = 21 , address = OFB

21 = 00100001 = STOR M(X)
= STOR M(OFB)

Hence assembly language code for
08C 020FA210FB is

LOAD - M(OFA)
STOR M(OFB)

b. 1. In 08A address, the M(OFA) transfer to the accumulator and transfer contents of accumulator to memory location OFB.

2. In 08B, address, the M(OFA) transfer to the accumulator and take next instruction from left half of M(08D).

3. In 08C address, the -M(OFA) transfer to accumulator and transfer contents of accumulator to memory location OFB.

Ans:(B)

- In memory address 2 can be load into the accumulator as follow;

  Opcode : 00000001

  Operand : 000000000010

- Two trips to memory for CPU needed to make to complete this instruction during the instruction cycle. CPU has to make access memory to fetch the instruction which contains the address of the data we want to load.

Ans:(C)

- Overall data paths to/from MBR is 40bits.
- Overall data paths to/from MAR is 12bits.
- All paths to/from AC is 40bits.
- All paths to/from MQ is 40bits.

[The END]