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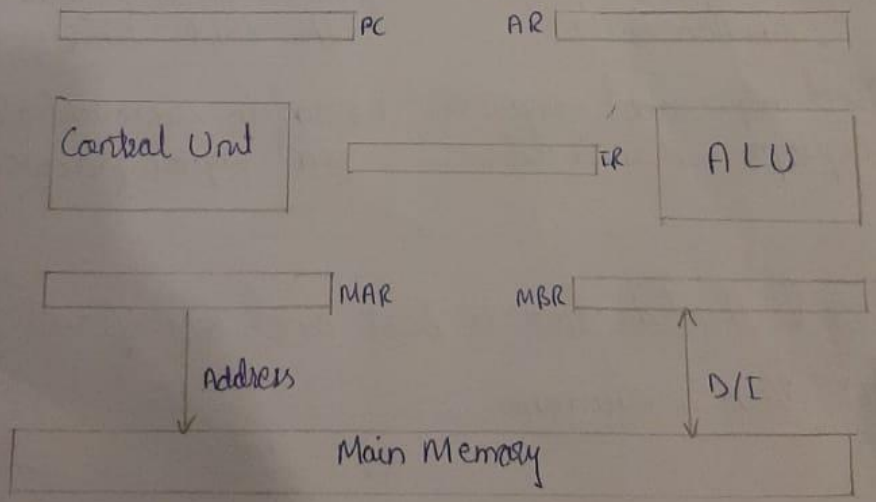
Advance Computer Architecture

Q1 a)

Illustration Instruction Set :-

OP	OPeration	Assembly Code	Effect	Time (ns)
000	Read	LOAD A	Mem[A] -> AR	2
001	Write	STOREA	AR -> Mem[A]	2
010	Addition	ADD A	AR + Mem[A] -> AR	2
011	Subtraction	SUB A	AR - Mem[A] -> AR	2
100	Branch	BRA A	A -> PC	1
101	Branch if not zero	BNZ	A -> PC if AR ≠ 0 ELSE PC + 1 -> PC	1
110	Input	IN	IN - Port - AR	1
111	Output	OUT	AR -> OUT - Port	1

Instruction Execution Mechanism :-



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Q1 (b)

	Von Neumann	Harvard Architecture
1.	It is theoratical design based on the stored-program computer concept	1. It is modern computer architecture based on the Harvard Mark I relay-based computer model.
2.	It uses same physical memory address for instructions and data	2. It uses separate memory addresses for instruction & data
3.	Processor needs two clock cycles to execute an instruction	3. Processor need one cycle to complete an instruction.
4.	Simpler control unit design and development of arr is cheaper and faster.	4. control Unit for two buses is more complicated which adds to the development cost
5	Data transfer & instruction fetches cannot be performed simultaneously	5. Data transfer and instruction fetches can be performed at the same time.
6.	Used in personal computers, Laptops and work stations	6. Used in microcontrollers and signal processing.

Harvard Architecture is best and is preferred more then Von-Neumann

Major Roles of CPU:

1. The primary function of a CPU is to execute the instruction stored in the main memory.
2. An instruction tells the CPU to perform one of its basic operation.
3. The CPU includes a set of registers which are temporary storage devices used to hold control information, key data, and intermediate results.
4. It includes also an internal bus infrastructure, which provides data movement paths among the control unit, ALU, and registers.
5. The CU is the one which interprets (decodes) the instructure to be executed and tells" the other components what to do.

Q2(a)

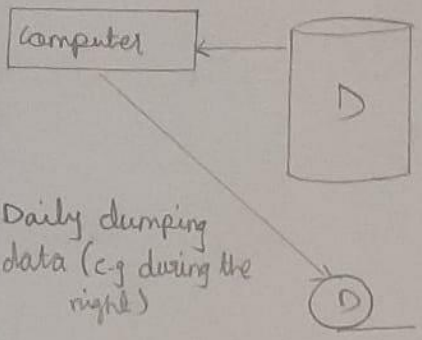
Machine Instructions :-

- Machine instructions specifies the following information
  1. What has to be done (operation code)
  2. To whome the operation applies (source operands)
  3. Where does the result go (destination operand)
  4. How to continue after the operation is finished (next instruction address).

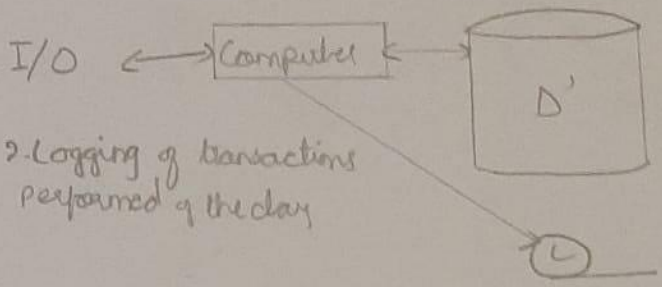
- Machine instructions are of four types.
  1. Arithmetic & logic operations.
  2. Data transfer between memory & CPU registers.
  3. Program control (e.g conditional branches)
  4. I/O transfer.

Q2a)

Back up Procedure

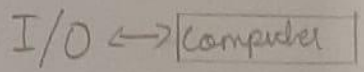


1. Daily dumping of data (e.g during the night)

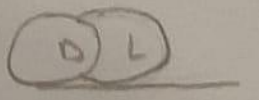


2. Logging of transactions performed of the day

3. Disk crashed happened



4. Your data are safe in the backup tapes



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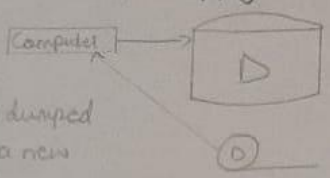
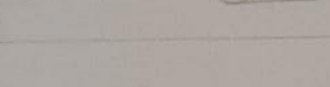
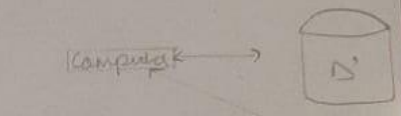
Back-up with Logging

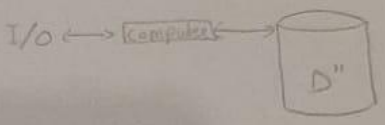


1. Copy the dumped data to a new disk

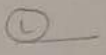




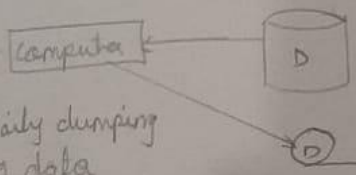
2. Update the dumped data with the logged transactions



3 The system is back to normal operation

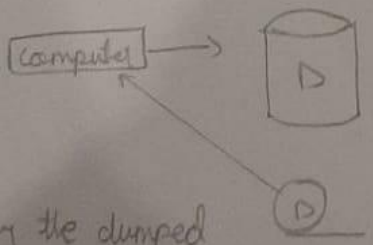


Back-up without Logging



1 Daily dumping of data

2. Disk crashed happens



3 Copy the dumped data to a new disk

Q2 b)

Memory Access Bottleneck

Quantitative measurement of the capacity of the bottleneck is the memory bandwidth.

- Memory bandwidth denotes the amount of data that can be accessed from a memory per second.

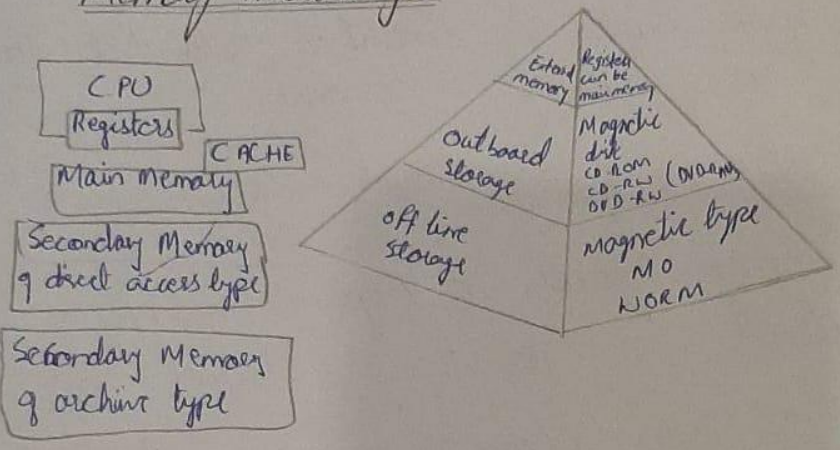
$$M\text{-}Bandwidth = \frac{1}{memory\ cycle\ time} \cdot amount\ of\ data\ per\ access$$

Ex. MCT = 100 nano second and 4 bytes (a word) per access.
M-Bandwidth = 40 mega bytes per second.

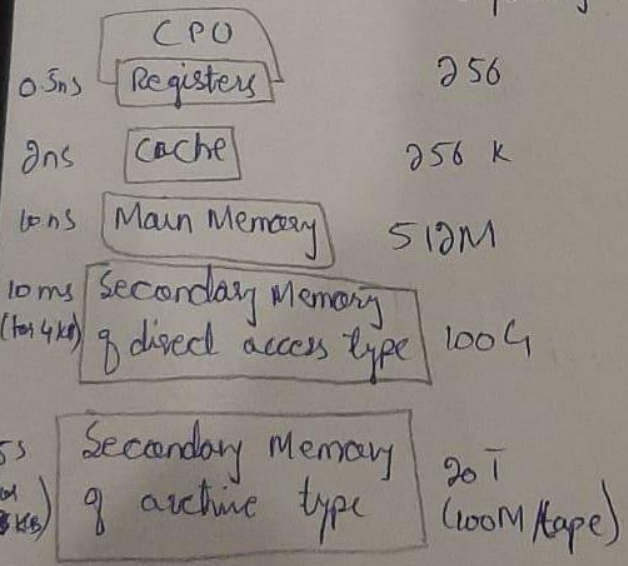
- There are two basic techniques to increase the bandwidth of a given memory.
  - Reduce the memory cycle time.
    - Expensive
    - Memory size limitation.
  - Divide the memory into several banks, each of which has its own control unit (using parallelism).

In computer architecture, the memory hierarchy separates computer storage into a hierarchy based on response time. Since response time, complexity, and capacity are related, the levels may also be distinguished by their performance and controlling technologies.

Memory Hierarchy:



Capacity example



As one goes down the hierarchy, the following occur:

- Decreasing cost/bit.
- Increasing capacity
- Increasing access time
- Decreasing frequency of access by CPU

Q2(c)

LOCALITY OF REFRENCE

- Programs access a small proportion of their address space at any short period of time.
- Temporal locality: If an item is accessed, it will tend to be accessed again soon.
- Spatial locality: If an item is accessed, items whose addresses are close by will tend to be accessed soon.
- This access pattern is an intrinsic features of the von Neumann architecture.
  - Sequential instruction storage and execution.
  - Loops and iterations (e.g subroutine calls).
  - Sequential data storage (e.g, array).

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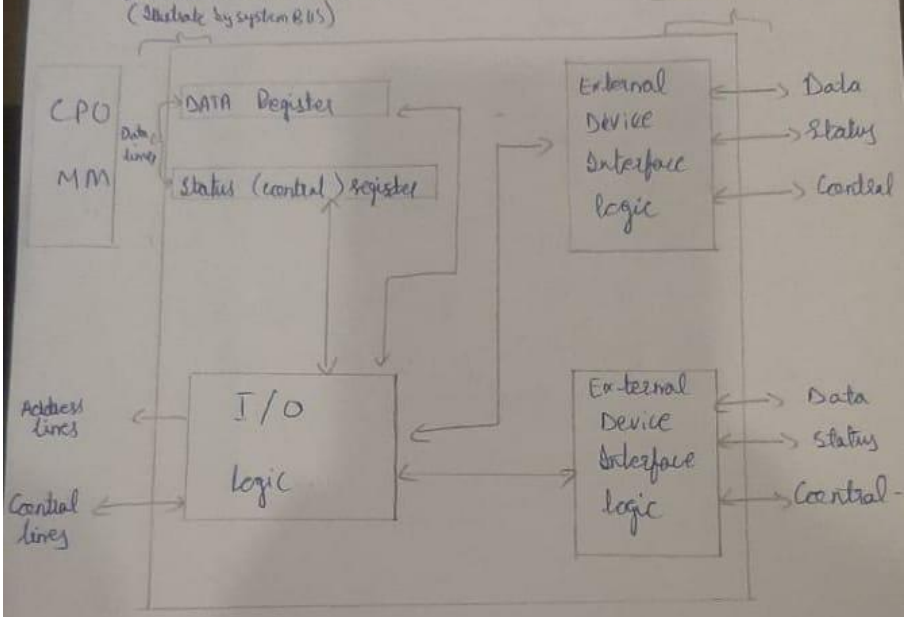
Q3 a)

Function of an I/O Module

-> Control and timing
-> CPU communication
-> Device communication (Interface by system BUS)
-> Data buffering
-> Error detection & Correction (Interface by system device)



Control of I/O Devices

Programmed I/O

- The operations are controlled by I/O instructions, for example, READ & WRITE.
- The instructions specify.
  - The particular I/O operations to perform; and
  - the given device by giving its address (its ID number)
- The CPU will wait for the I/O operation to be finished before it executes the next instructions.
- Since the I/O devices are very slow, the CPU has to wait all the time instead of doing useful work.
- It is very simple but not an efficient method.
  - can be used in embedded system.

Q3 b)

B.S = 4

T. check = 2.1m

P. ht = 0.97

MAT will be 25ns.