Department of Electrical Engineering
Assignment
Date: 20/04/2020

Course Details

Course Title: VLSI **Module:** 6th

Instructor: Engr. Zulqarnain **Total Marks:** _____

Student Details

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Part A (Objective Type)

1. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance??
   a. Static dissipation
   b. Dynamic dissipation ✓
   c. Both a and b
   d. None of the above.

2. Which type of MOSFETS Exhibits no current at zero gate voltage?
   a. Depletion MOSFET
   b. Enhancement MOSFET ✓
   c. Both a and b
   d. None of the above

3. CMOS circuits are constructed in such a way that all PMOS transistors must have either an input from the voltage source or from another
   a. PMOS transistor ✓
   b. NMOS transistor
   c. CMOS transistor
   d. BJT transistor

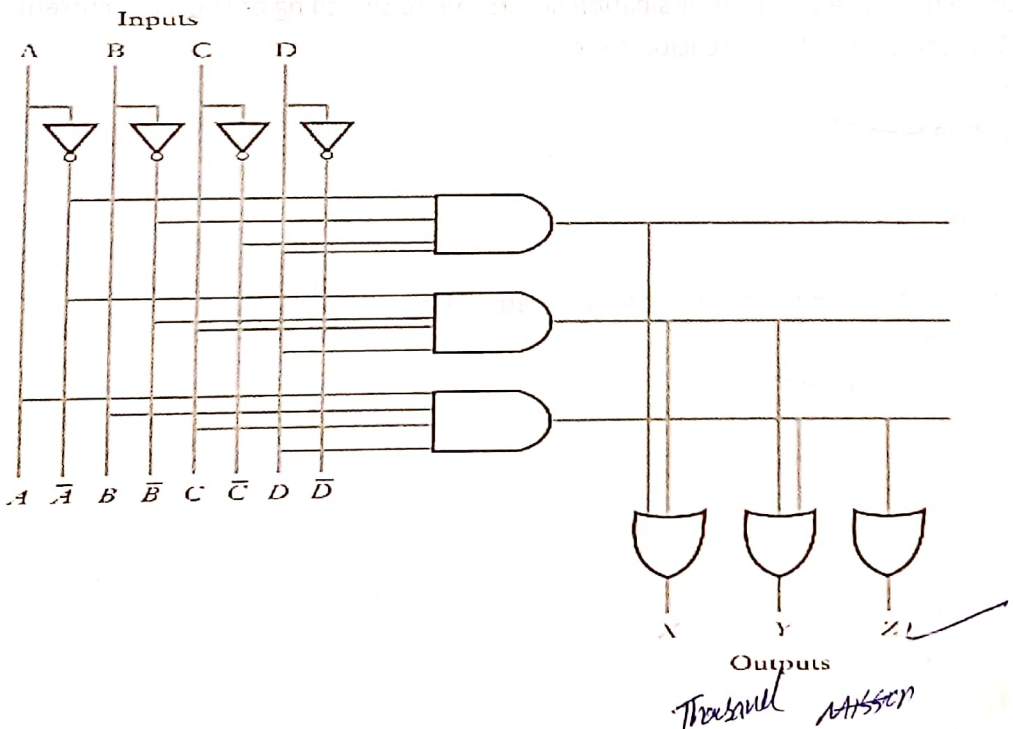
4. Delay which is equal to the time taken by a gate output transition to 0, from another value 1, x, or z is
   a. Rise delay
   b. Fall delay ✓
   c. Turn-off delay
   d. Turn-on delay

5. Which type of simulation model is used to check the timming performance of a design?
   a. Transistor level
   b. Gate level
   c. Behavioral
   d. Switch level
   e. None of these

6. Which of the following statements is incorrect
   a. Some PLDs are programmed using electrically operated switches.
   b. Some PLDs are programmed using mechanical switches

Fill in the Blanks

7. In MOS devices, the current at any instant of time is constant and independent of the voltage across their terminals.
8. For complex gate design in CMOS, OR function needs to be implemented by parallel connections of MOS
9. In the following PLA, which output implements the logic function ABCD??



10. The term VLSI means a device containing between ____ and_____ transistors.

Million

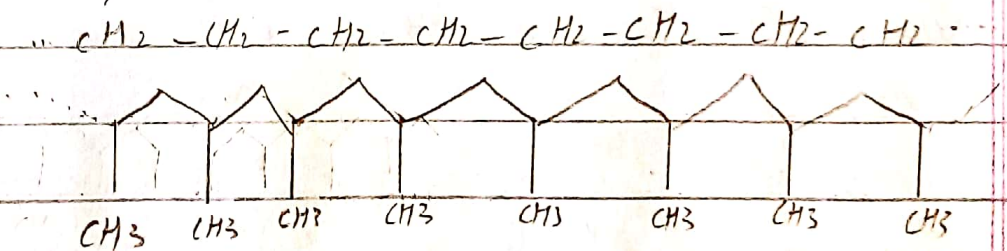
Q1 In lower low lower VLSI design clock gating technique will reduce power all time or it depends upon the input data? In any chance the computation power may increase?

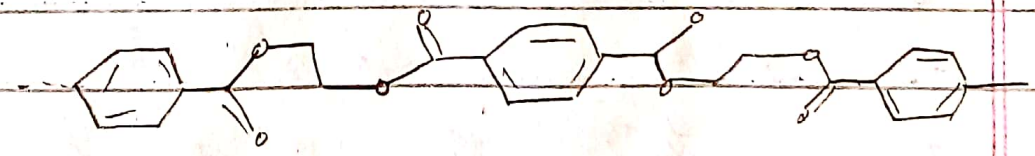
Ans. Using this clock-gating technique the flip-flop clock only when the output has to change. clearly this mean that the flop will clock less this circuit than in the previous one.

In reality when this is done via the synthesis tool rather than just an 'and' gate a latch integrated cell in the library is used with the and to prevent glitch issues when the timming of the clock and enable are different (clock-tree synthesis) there may also be added observability for DFT reasons. clearly a gating structure would not be applied to every register since science the cost in power of the gating would exceed the saving on a flop.

Q2 B) While fabrication of NMOS or PMOS we usually use inorganic polymer. If we use organic polymer instead of inorganic polymer what will happen?

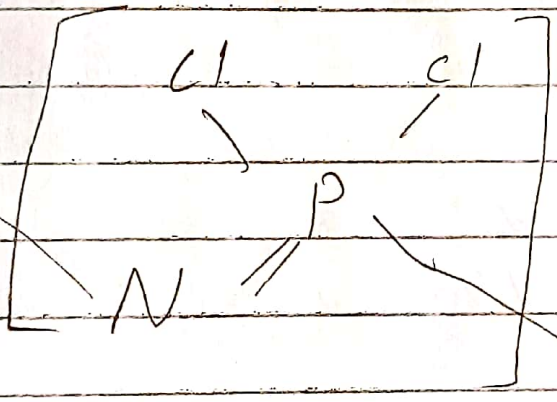
Ans. Organic polymers are polyme materials that essentially contain carbon atoms in the backbone. Therefore there are only carbon covalent bond in these. These polymers form only from organic monomer molecules. Most of the times, these polymers are environmental friendly since these are biodegradable.





Furthermore these are two major forms of organic polymers such as natural and synthetic polymers. Common example of important organic polymers include polysaccharide proteins, polynucleotides (DNA and RNA) etc.

Inorganic polymers are polymer materials that have no carbon atoms in the backbone. However, most of these are some organic regions as well. These materials are highly branched structures and have chemical element other than carbon e.g. sulfur nitrogen.



Moreover, these polymers are not environmentally friendly because they are not biodegradable. Some common example include polydimethesiloxane (silicon rubber) polyphosphazens etc.

(Q2a) If we want to design an IC and I want that each every transistor used in this IC should be optimized individually with less time. How it will be possible?

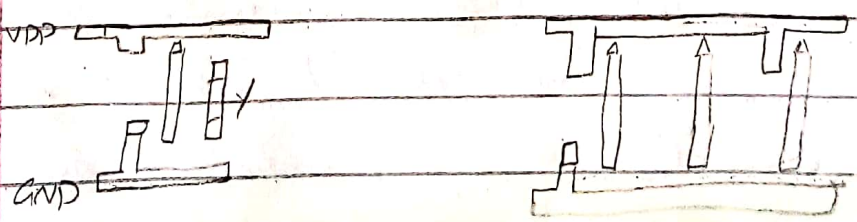
Ans: A transistor is a semiconductor device used to amplify or switch electronic signals and electrical power. It is composed

of semiconductor material usually with at least three terminals for connection to an external circuit. A voltage or current applied to one pair of the transistor terminal control the current through another pair of terminal. Because the control (output) power can be higher than the controlling (input) power a transistor can simplify a signal. Today some transistor are packed individually but many more are found embedded in integrated circuit.

Q3 Draw a stick diagram of a layout using that veriable ordering. F = ACD + ABD

Ans. Stick Diagrams.

Stick diagrams help plan layout quickly
- Need not be to scale
- Draw with color pencil or dry-erase markers.



a)

~~Wiring~~ Wiring

Wiring Tracks

→ A wiring track is the space required for a wire of 1 width 4x spacing from neighbor = 8 1 pitch

→ Transistor also consume one wiring track

* Well spacing

Wells must surround transistor by 6 1

- implies 12 1 between opposite transistor flavors
- Leaves room for one wire track.

Area Estimation

Estimate area by counting wiring tracks

Multiply by 8 to express in 1.