**Department of Electrical Engineering**
**Assignment**
**Date: 20/04/2020**

**Course Details**

**Course Title:** VLSI Technology **Module:** 6th
**Instructor:** Engr. Zulqranin Abbasi **Total Marks:** 30

**Student Details**

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Part A (Objective Type)

1. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance??

a. Static dissipation

✓ b. Dynamic dissipation

c. Both a and b

d. None of the above.

2. Which type of MOSFETS Exhibits no current at zero gate voltage?

a. Depletion MOSFET

✓ b. Enhancement MOSFET

c. Both a and b

d. None of the above

3. CMOS circuits are constructed in such a way that all PMOS transistors must have either an input from the voltage source or from another

✓ a. PMOS transistor

b. NMOS transistor

c. CMOS transistor

d. BJT transistor

4. Delay which is equal to the time taken by a gate output transition to 0, from another value 1, x, or z is

   a. Rise delay

   b. Fall delay

   c. Turn-off delay

   d. Turn-on delay

5. Which type of simulation model is used to check the timming performance of a design?

   a. Transistor level

   b. Gate level

   c. Behavioral

   d. Switch level

   e. None of these

6. Which of the following statements is incorrect

   a. Some PLDs are programmed using electrically operated switches.

   b. Some PLDs are programmed using mechanical switches

Fill in the Blanks

7. In MOS devices, the current at any instant of time is _____ of the voltage across their terminals.

   constant & Independent

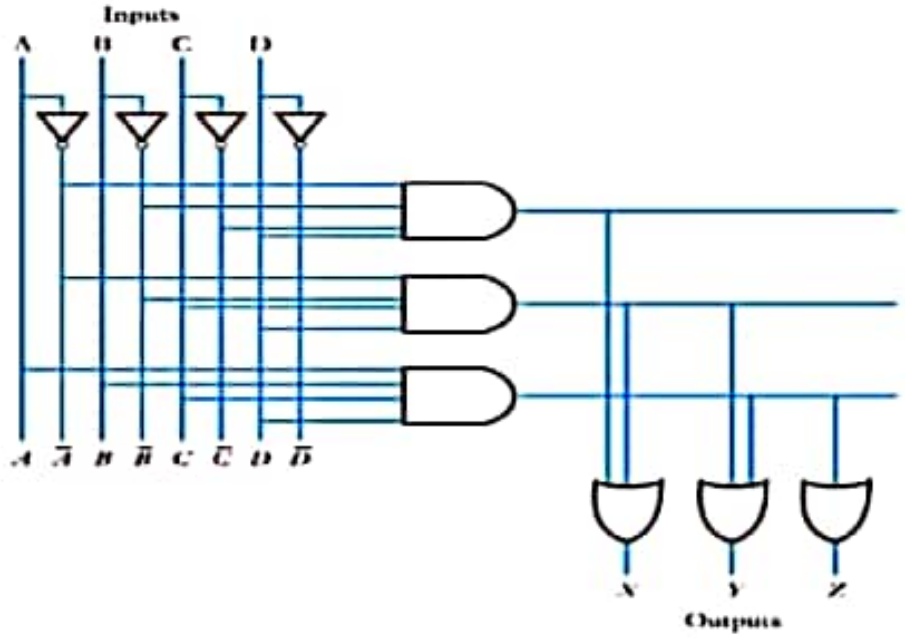
8. For complex gate design in CMOS, OR function needs to be implemented by _____ connections of MOS

   parallel

9. In the following PLA, which output implements the logic function ABCD??

Ans:-

The output Implements of the logic function is Z




10. The term VLSI means a device containing between ____ and_____ translstors.

Thousands & Million

## Q No :- 1

**Ans :-**

### Low power VLSI design clock gating technique will reduce power all time:-

The clock gating technique is basically used for decreasing the dynamic power reduction. After applying this technique the main problem will be

1) the no. of transistor count will increase

2) the revised or modified circuit may require variable voltage sources which leads to some DC -DC conversion circuits may require which leads to more complexity of the circuit

3) no of interconnect capacitance increase and hence delay may increase

4) Static power may increase

So, mainly it sole responsible of the designer to use this technique judicially to affect the above factors to a minimal level.

### point 2 that clock gating may require variable voltage sources?

In this case.if clock gating is properly used the benefits will be much greater than the drawbacks.

Using this clock-gating technique, the flip-flop clocks only when the output has to change. Clearly this means that the flop will clock less in this circuit than in the previous one.

In reality when this is done the synthesis tool, rather than just an "and" gate, a latch (integrated cell in the library) is used with the "and" to prevent glitch issues when the timing of the clock and enable are different (clock-tree synthesis), there may also be added "observability" for DfT reasons.

Clearly, a gating structure would not be applied to every register (since the cost in power of the gating would exceed the saving on a flop).

Q No :- 2 part (A)

Ans :-

## Integrated circuit design :-

IC design, is a subset of electronics engineering, encompassing the particular logic and circuit design techniques required to design integrated circuits, or ICs. ICs consist of miniaturized electronic components built into an electrical network on a monolithic semiconductor substrate by photolithography.

**IC design can be divided into the broad categories :-**

- **Analog**
- **digital**

## Analog :-

Analog IC design is used in the design of **op-amps, linear regulators, phase locked loops, oscillators** and **active filters.** Analog design is more concerned with the physics of the semiconductor devices such as **gain, matching, power dissipation,** and **resistance.** Fidelity of analog signal amplification and filtering is usually critical and as a result -

- analog ICs use larger area active devices

## Digital :-

Digital IC design is to produce components such as **microprocessors, FPGAs, memories (RAM, ROM, and flash) and digital ASICs.** Digital design focuses on logical correctness, maximizing circuit density, and placing circuits so that clock and timing signals are routed efficiently. Analog IC design also has specializations in power IC design and RF IC design.

- digital designs and are usually less dense in circuitry.

**transistor are used in every IC :-**

the number of transistors is used in every IC started to increase exponentially. In fact, in 2006, chips were created that contained up to 100 million transistors per square centimeter.

**Or**

The number of transistors has thus been changing over the years. In the 1970s, an IC might have approximately 3,000 transistors. Now, the number of transistors has reached 42 million.

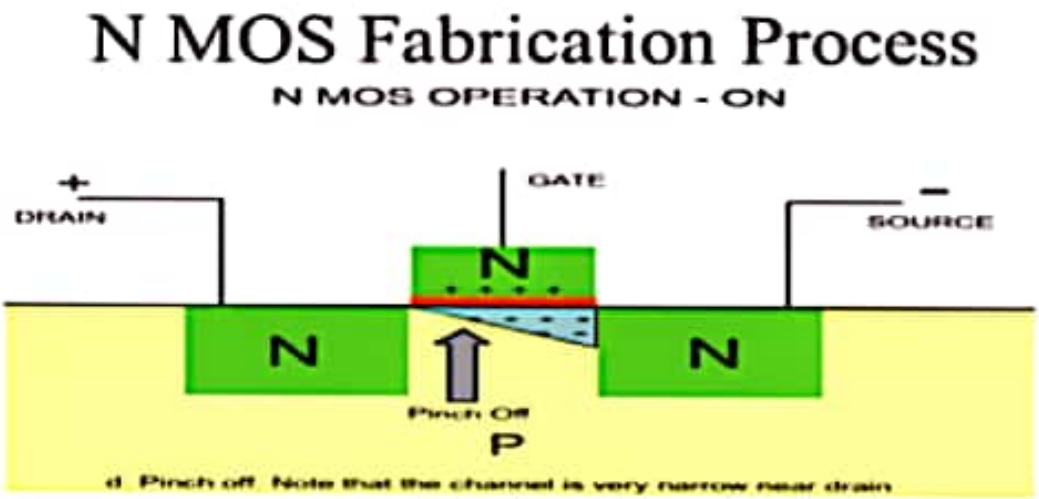
**It can be possible :-**

Integrated circuits are found in every technological device that we use today, from computers and calculators to watches and cellular phones. An integrated circuit (IC) is a tiny silicon chip, less than a centimeter in width. Among other things, the IC contains arrays of transistors that help process data. The more transistors there are in a circuit, the faster the data is processed. Modern technology has allowed data to be processed rapidly by increasing the number of transistors and decreasing the size of the IC.

Q No :- 2 (part : B)

**Ans :- NMOS or PMOS Fabrication Process:-**

There are a huge number and assortment of fundamental fabrication steps utilized as a part of the generation of present-day MOS ICs. A similar procedure can be utilized for the planned of NMOS or PMOS or CMOS devices. The most commonly used material could be either metal or poly-silicon. The most regularly utilized substrate is mass silicon or silicon-on-sapphire (SOS). In order to keep a strategic distance from the nearness of parasitic transistors, varieties are acquired the systems that are utilized to isolate the devices in the wafer. The NMOS fabrication steps are as per the following.




**NMOS Fabrication Steps:-**

Using the fundamental processes, usual processing steps of the poly-Si gate self-aligning nMOS technology are discussed below. It can be superior understood by allowing for the fabrication of a single enhancement-type transistor. The step by step procedure of NMOS fabrication steps include the following

**Step1:**

Processing is passed on single crystal Si of high purity on which necessary P impurities is initiated as the crystal is developed. The diameter of such wafers are about 75-150 mm and 0.4 mm thick and they are doped with say boron to impurity absorption of 10 to power 15/cm3 to 10 to the power 16 /cm3.

**Step2:**

A SiO2 (silicon dioxide) layer normally 1 micrometer broad is grown all above the exterior of the wafer to guard the surface, performs as a barrier to the dopant through processing, and offers a generally protecting substrate on to which extra layers may be deposited and decorative.

**Step 3:**

The exterior (surface) is now enclosed with the photo oppose which is deposit onto the wafer and spun to an even distribution of the necessary thickness.

**Step 4:**

The photoresist coating is then uncovered to ultraviolet (UV) light through masking which describes those areas into which transmission is to take place as one with transistor channels. Suppose, for example, that those areas uncovered to UV radiations are polymerized, but that the areas necessary for diffusion are protected by the cover and remain unchanged.

**Step 5:**

These regions are consequently readily fixed away together with the original silicon-di-oxide so that the surface of the wafer is uncovered in the window defined by the mask.

**Step 6:**

A thin layer of SiO2 (0.1 micro m typical) is grown over the chip surface after removing the remains of photoresist. Further, a gate structure is created by depositing polysilicon on the top of it. Factors like precise control of thickness, impurity concentration, and resistivity are necessary for the fabrication of fine pattern devices.

**Step 7:**

Further, the photoresist coating and masking allows the polysilicon to be patterned. After this, the thin oxide is removed to expose the areas. These areas are defused with n-type impurities by heating the wafer to a high temperature and passing the gas of desired n-type impurities to form the source and the drain.

**Note: The polysilicon has an underlying thin oxide which acts as a mask during diffusion. This is called self-aligning.**

**Step 8:**

Again a thick oxide of SiO2 is grown over and then masked with photoresist. Now it is etched to expose selected areas of the polysilicon gate, drain and the source where connections are to be made.

**Uses of Nmos or Pmos :-**

PMOS transistor may use a material with ... for the NMOS transistors and 15 Angstroms for the gate dielectric for PMOS transistors ... For example, materials for the NMOS transistor, such as silicon dioxide, may be deposited using ...

**organic-Inorganic polymer :-**

, polymer LED displays are use candidates for all display applications from simple segmented displays (such as are used in watches and

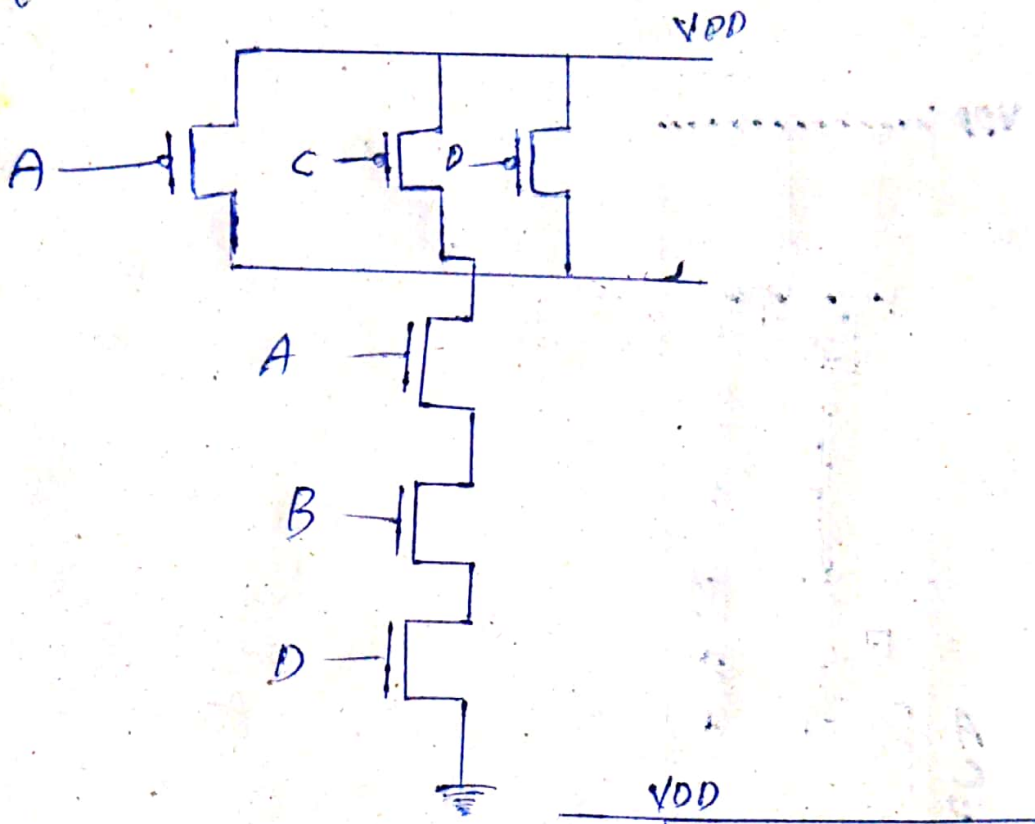
n-type or p-type organic semiconductors can realize unipolar logic circuits in a similar way to the NMOS (n-type metal-oxide semiconductor) or PMOS (p-type metal ... To fabricate a CMOS-like circuitry, the use of both p-channel and n-channel OTFTs with matching mobilities is

**Q No:-3:-** Draw a stick diagram of a layout using that Variable ordering

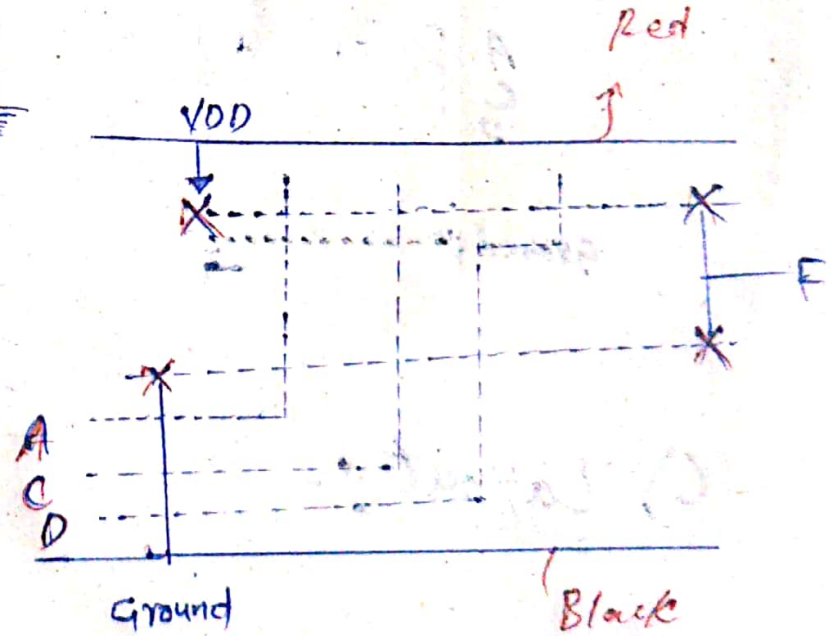
$$F = ACD + ABD$$

**Ans:-**

$$F = ACD + ABD$$




a) Schematic



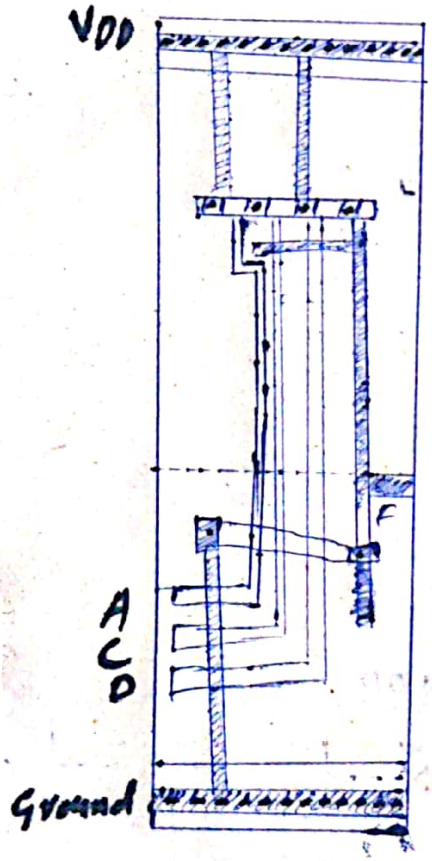

b) Stick diagram

→ VDD = are Red cable used

→ ground = are Black cable is used

→ Connection are Yellow colour is used

→




## c) Layout :-