

Digital Logic Design

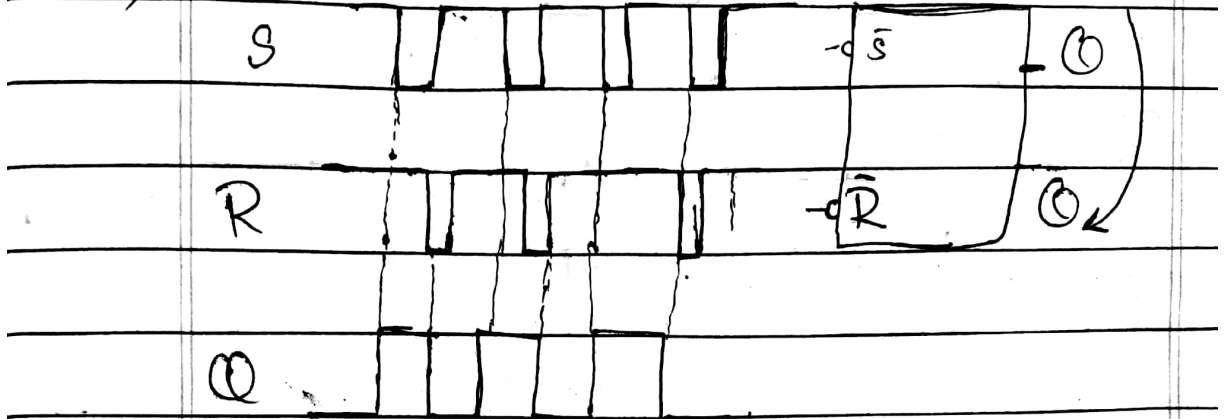
Six-Muhammad Amin

Muhammad Yasir

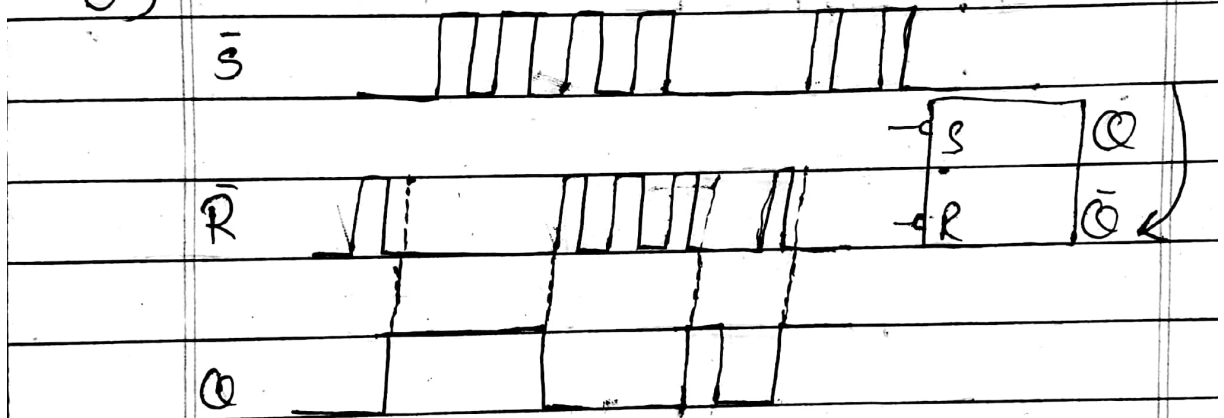
15459

Assignment # 06

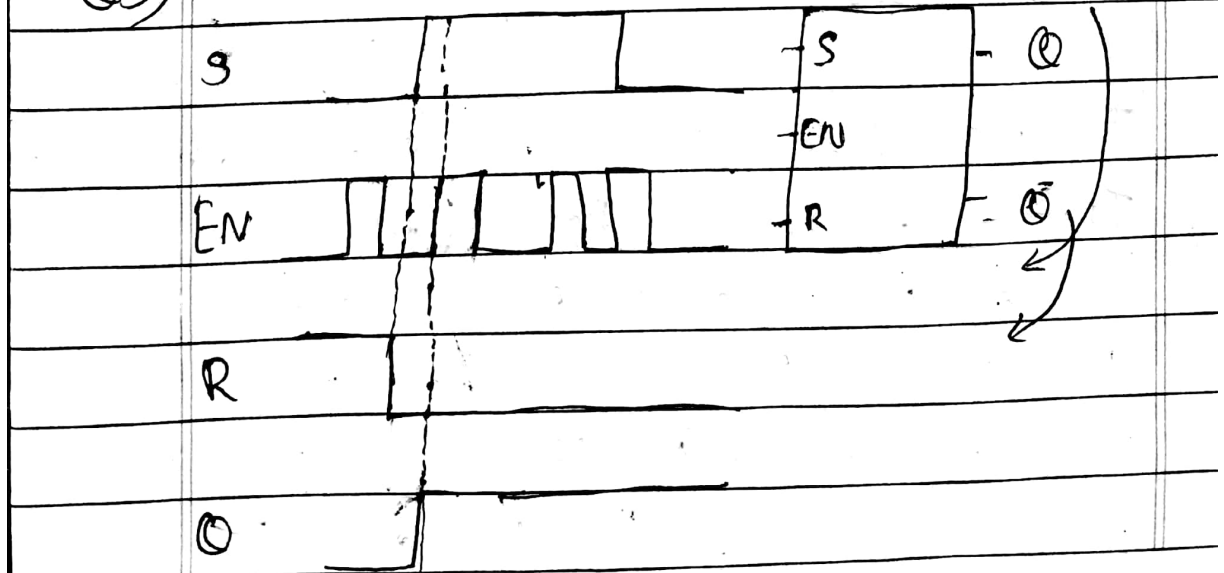
Q1)



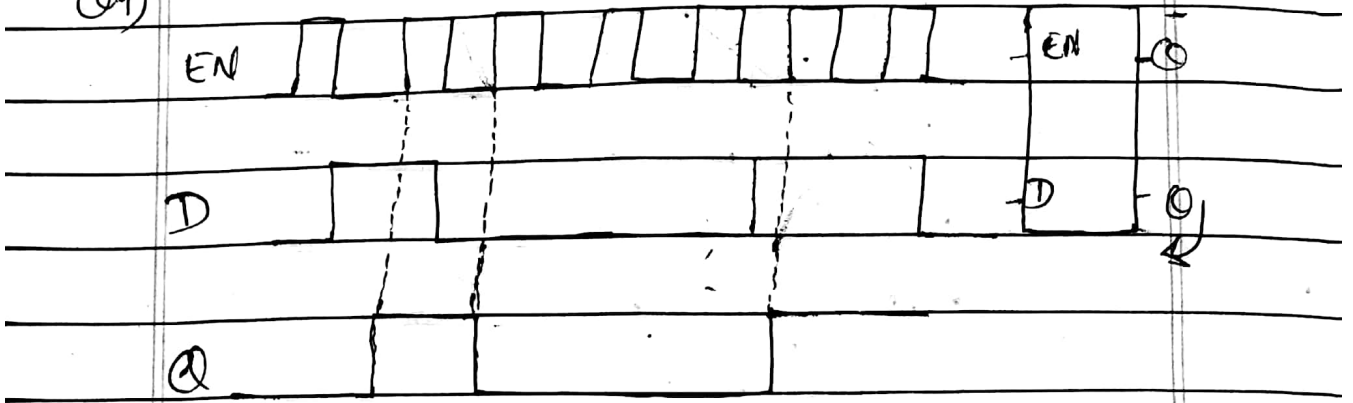
Q2)



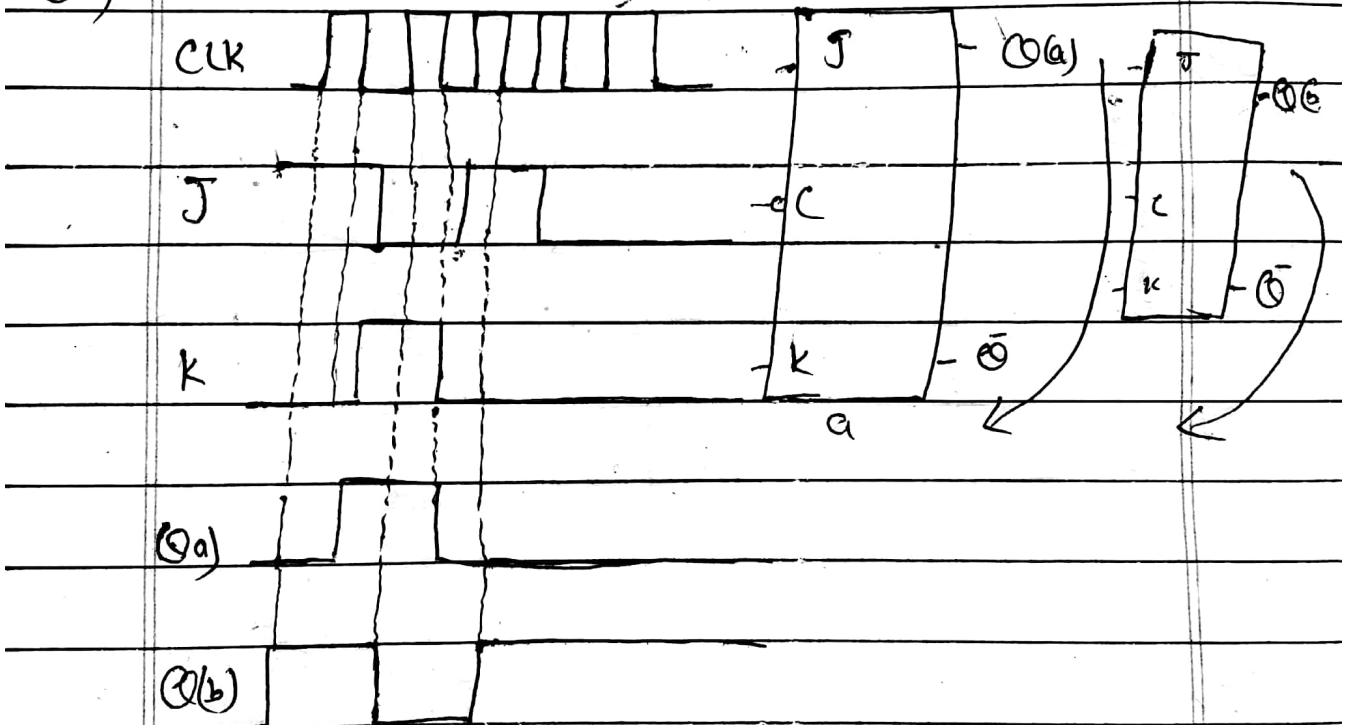
Q3)



(Q4)



(Q5)



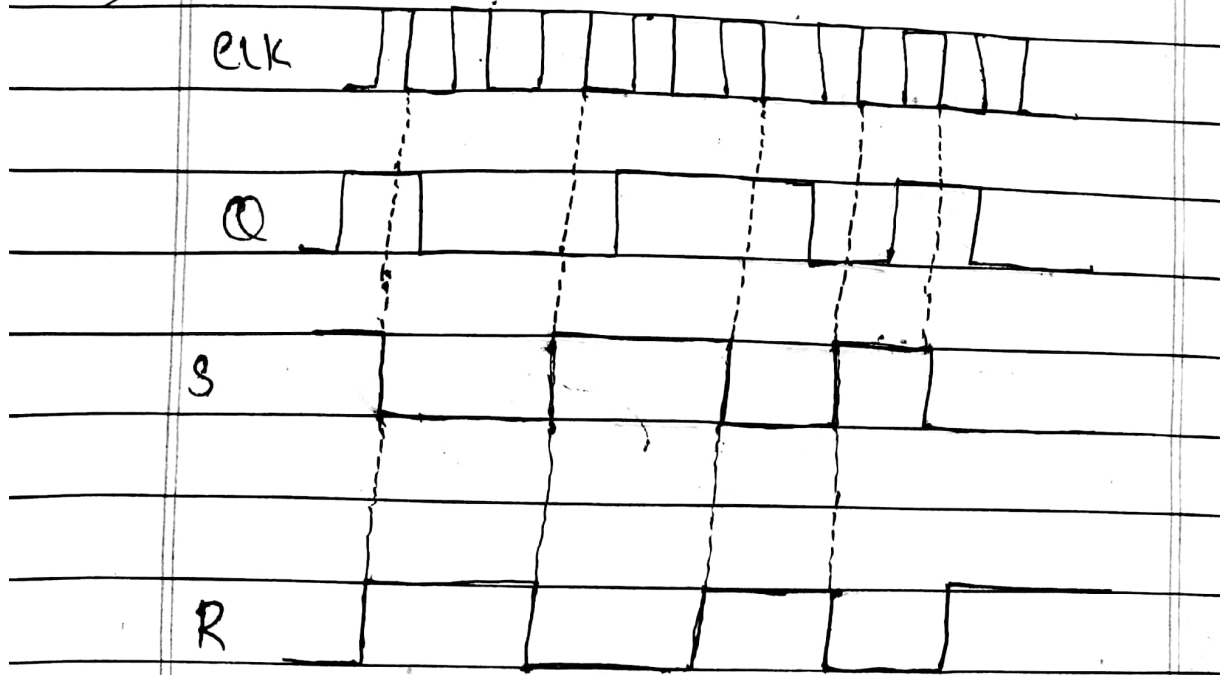
The main difference b/w (a) & (b) edge triggered

J-K flip-flops is that triggers

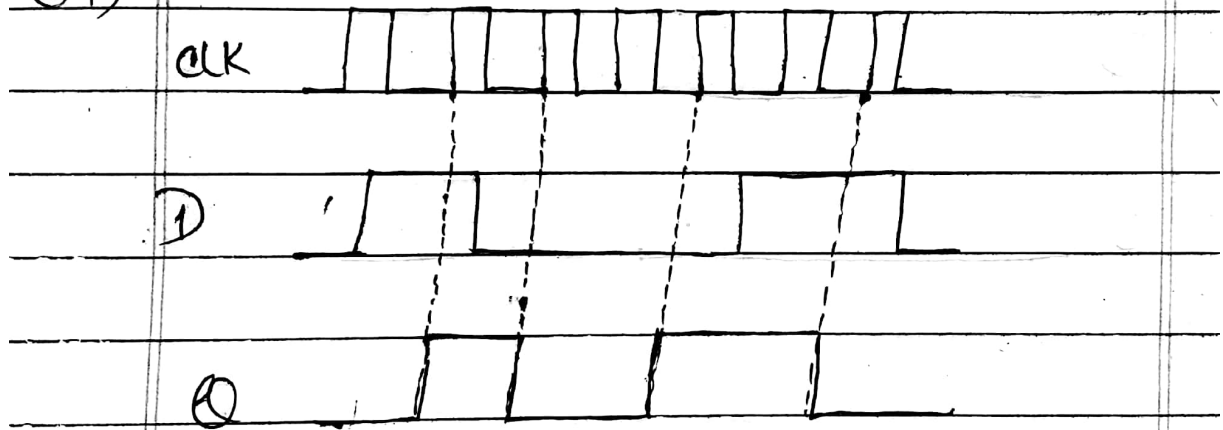
The flip flop (a) on the negative edge of the clock pulse, while

The flip flop (b) triggers on the positive edge of the clock pulse.

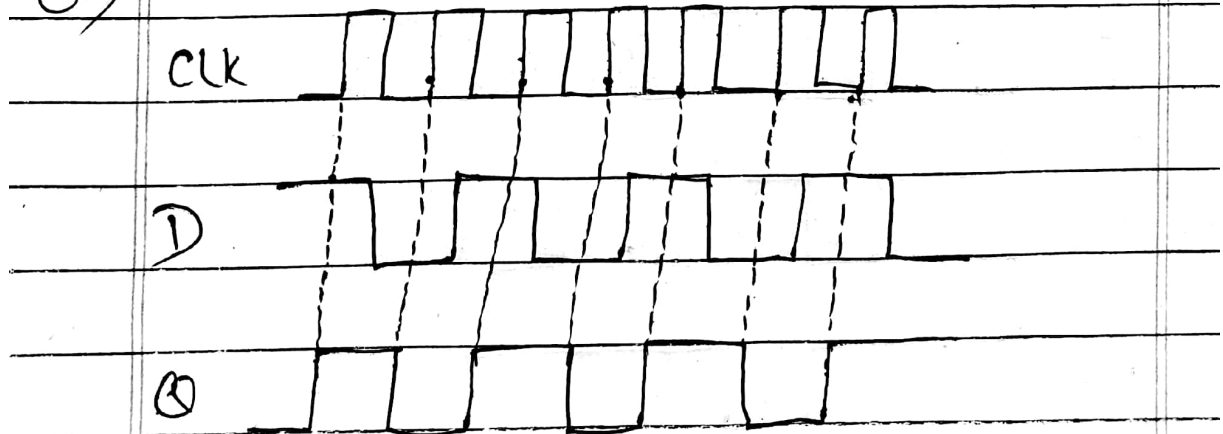
(06)



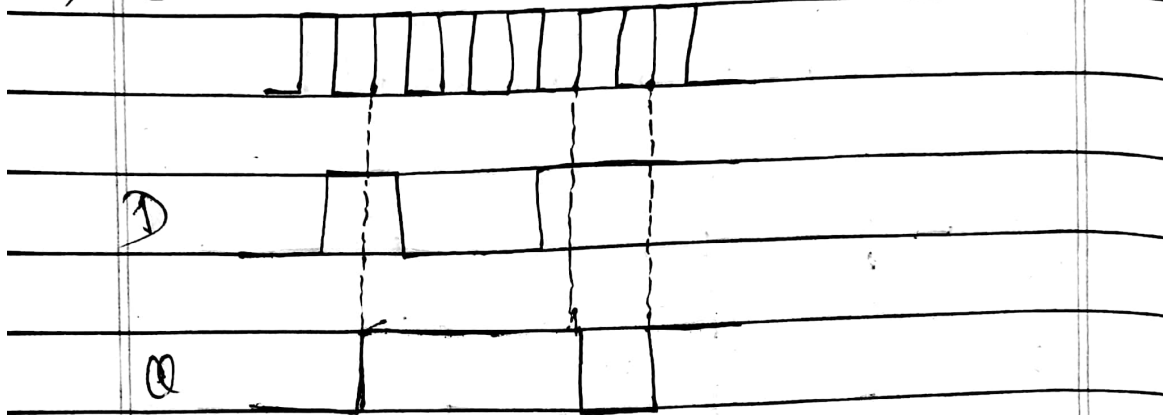
(07)



(08)

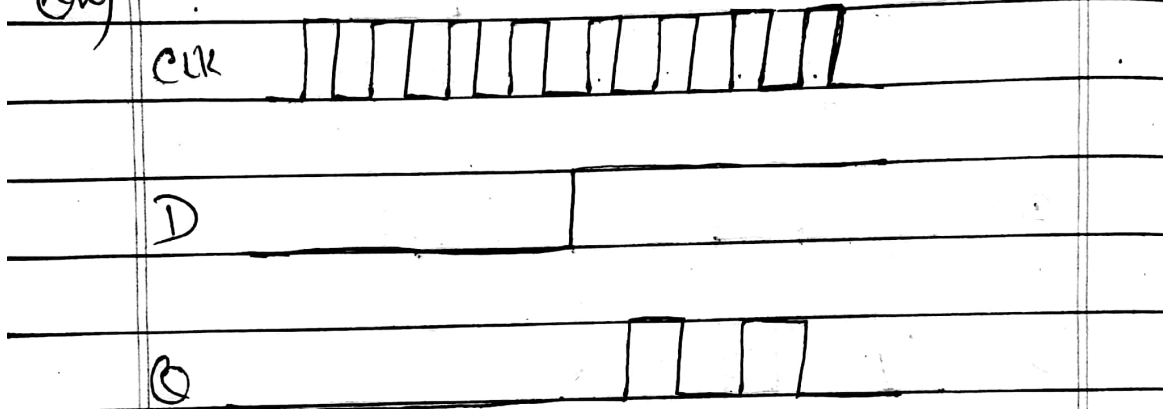


Q1) CLK

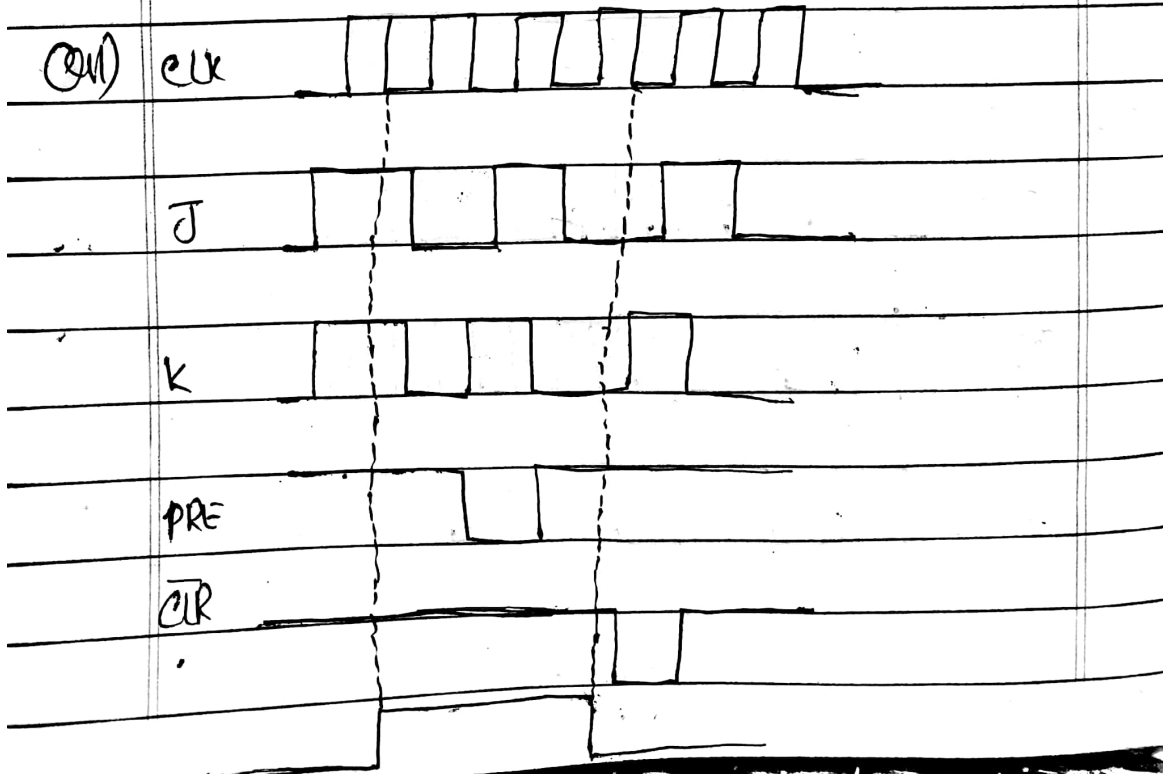


Q2)

CLK



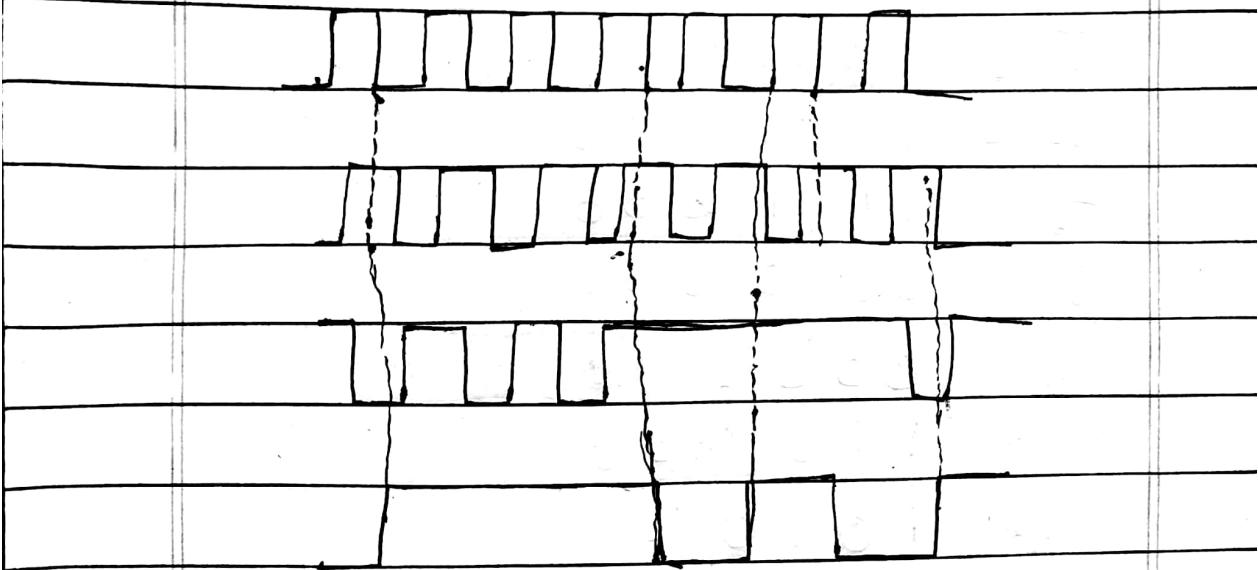
Q3) CLK



Date

Day

(10)



(11) CLK

PRE

J₁

J₂

J₃

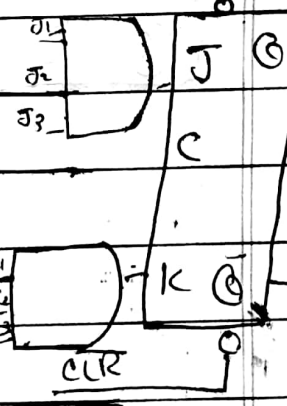
K₁

K₂

K₃

Q₁

Q₂



(Q13)

$$J_1 = 1010011$$

$$J_2 = 0111010$$

$$J_3 = 1111000$$

$$J = 0010000$$

$$K_1 = 0001110$$

$$K_2 = 1101100$$

$$K_3 = 1010101$$

$$K = 0000100$$

$$J = 0010000$$

$$K = 0000100$$

$$\textcircled{0} = 0011000$$

Date

--	--	--	--	--	--	--	--	--	--

Day

M	T	W	T	F	S
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(Q15)

CLK

J₁

J₂

J₃

K₁

K₂

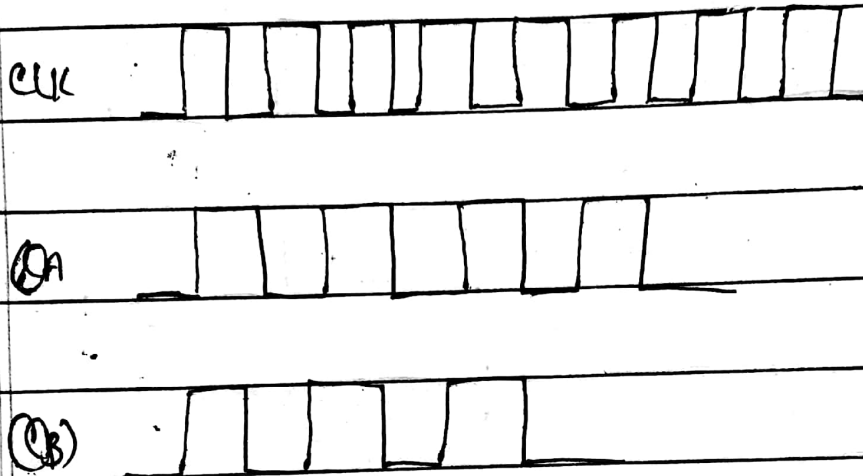
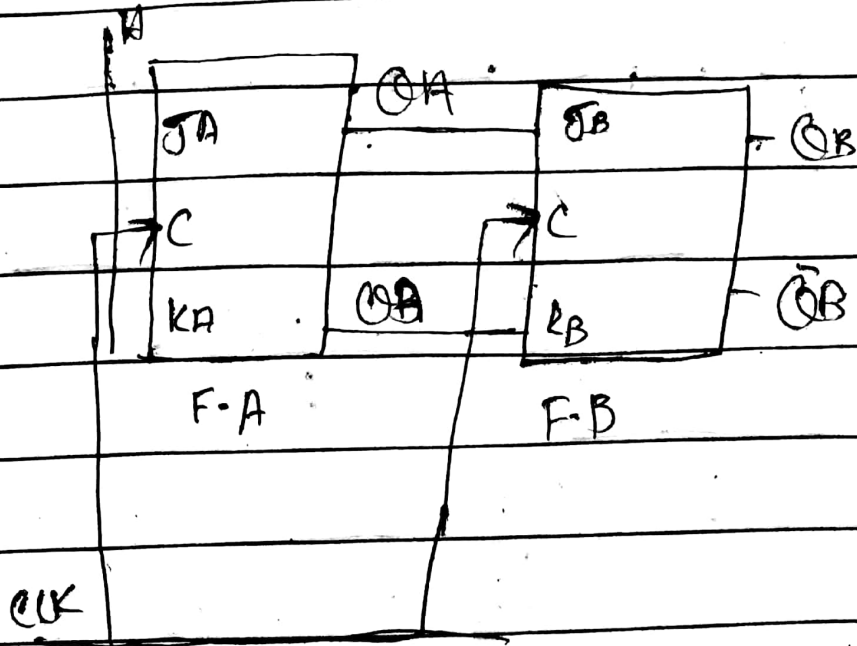
K₃

PRE

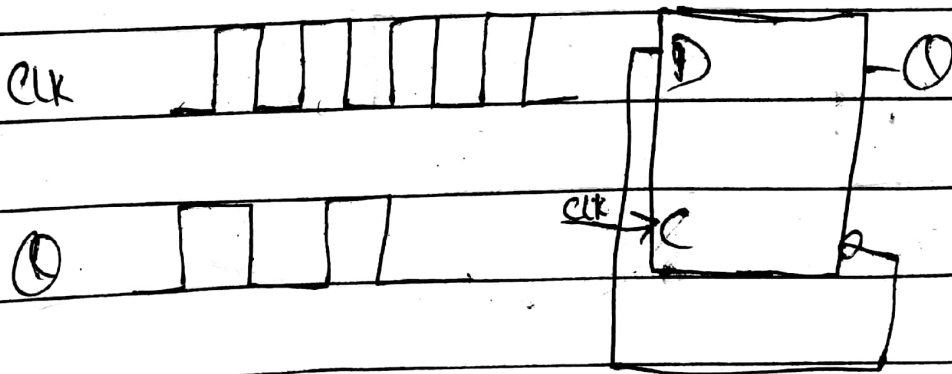
CLR

Q

(Q6)

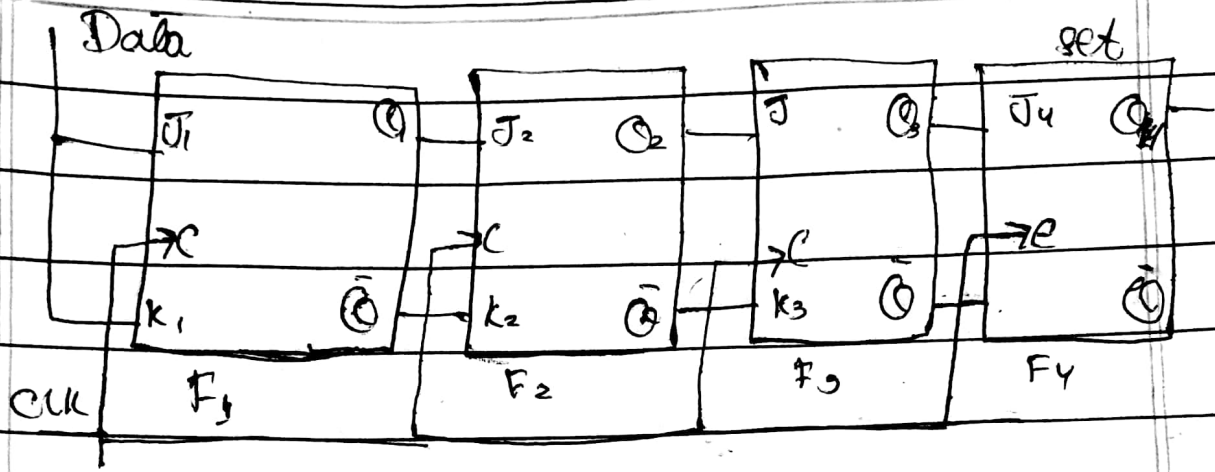


(Q7)



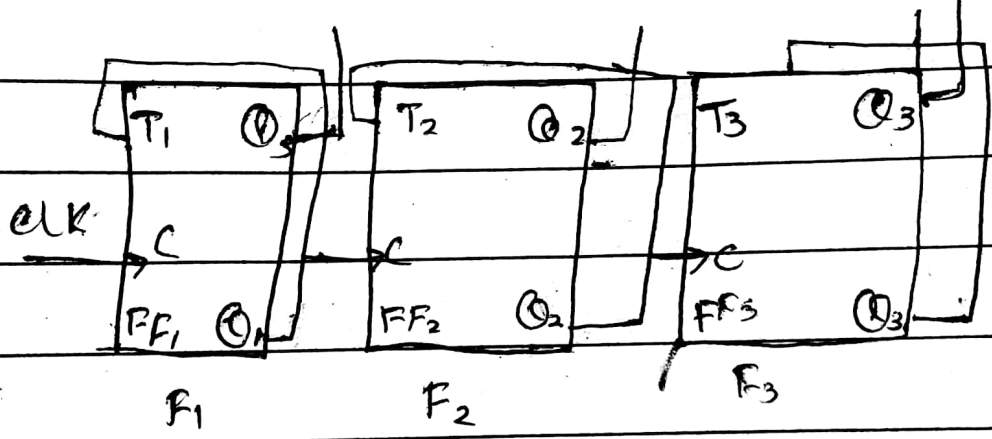
The device performs the divide-by-two function.

(Q18)



(Q19)

$\textcircled{A} = f/2$ $\textcircled{B} = f/4$ $\textcircled{C} = f/8$



Here if the input frequency is 8 kHz then at given marks frequency will be as follows.

$\textcircled{A} = f/2 = 4\text{ kHz}$

$\textcircled{B} = f/4 = 2\text{ kHz}$

$\textcircled{C} = f/8 = 1\text{ kHz}$