Name=Wair Page (1) ID=1909

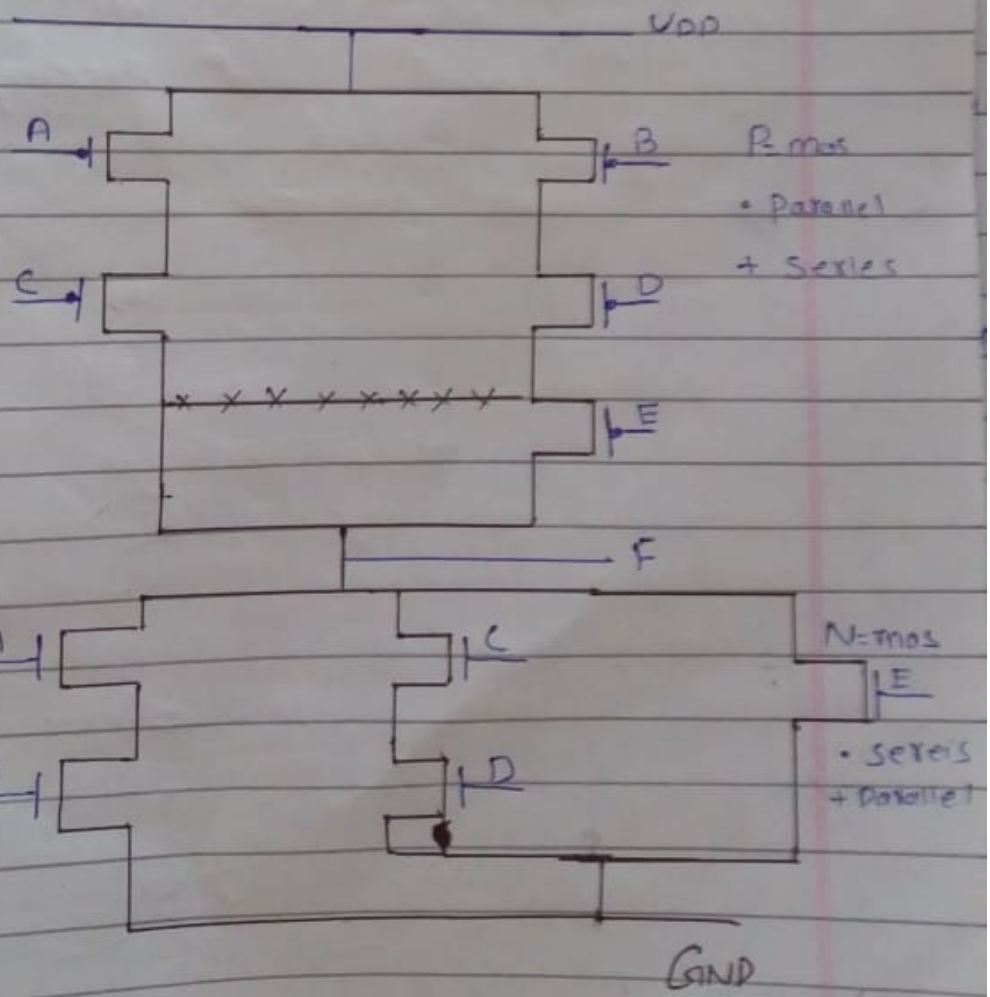
(1) Design an area efficient layout diagram for the cmos Logic shown below

F = AB + (CD) E

ns:-

N = . Series
+ Parallel

P = . Parallel
+ Series

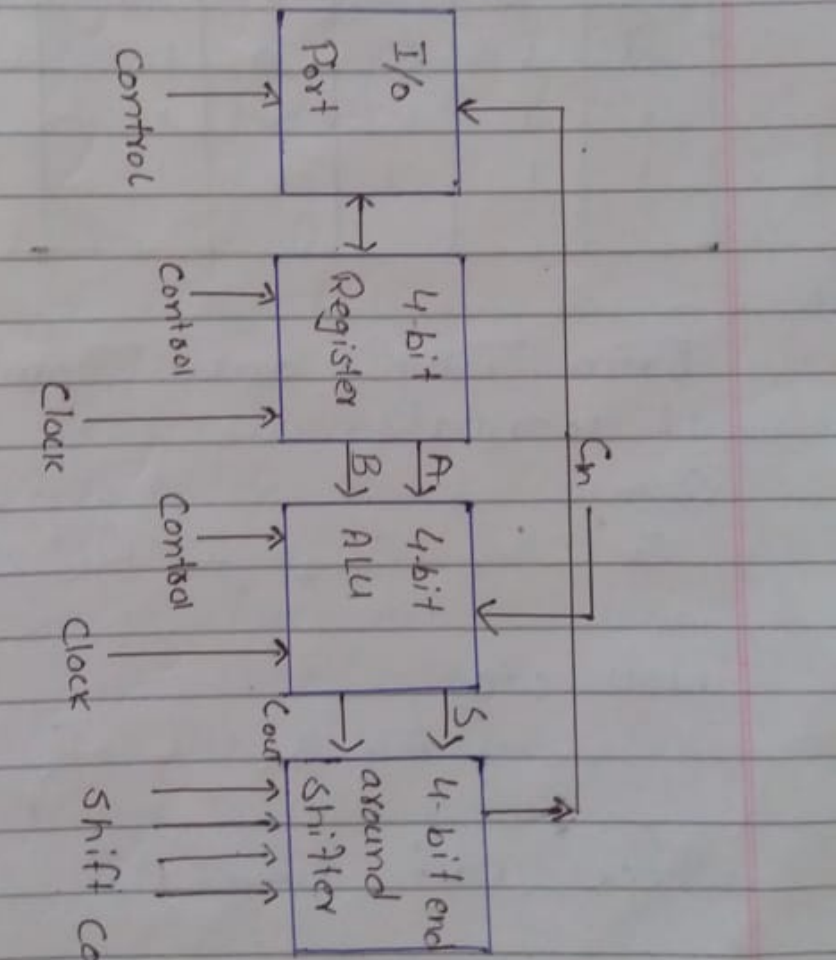


Name- Uzair Page (2) ID: 13909

Q(2) Give the Subsystem design consideration of a four-bit adder.

Ans

Now I want to design an Subsystem design consideration of a four bit adder.



=> Design of 4- bit adder

Inputs			outputs	
A_K	B_K	C_{K-1}	S_K	C_K
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

From Table one form of the equation is:

Sum

$$S_K = H_K C_{K-1}' + H_K' C_{K-1}$$

New carry

$$C_K = A_K B_K + H_K C_{K-1}$$

where Half Sum

$$H_K = A_K' B_K + A_K B_K'$$

Q(3) Discuss the VLSI issues and design Trend.

Ans First of all I want to discuss about VLSI design issues.
So

=> The VLSI design issues:

=> Realize a given specification on silicon, optimizing the following features

=> Area (yield)
=> Power dissipation
=> Speed
=> design time
=> Testability

=> optimization cannot be done in one step
=> partition Problem & optimize Subproblems.

Name: Uzair Page(s) ID=13909

=> Now I'm discussing about VLSI design Trends.

=> The Trend in design & manufacturing of very Large Scale integrated CICT shows an ongoing move Towards Smaller devices on increasing wafer dimensions CMOS has became the prevailing Technology due to it's high speed and packing density coupled with Low power consuption.

=> There are several Trends in VLSI design processor, memory, iss devices, Computer hardware & software. Telecamunications, Databases and ware houses etc.

Name=Wajiz Page(6) ID=13909

Q(3) (B)

Explain with neat diagram Simple parity check code.

Ans= An parity check code is the process that ensures accurate data Transmission b/w node during Communication. A parity bit appended to signal Signal bit to create an even or odd bit number the number bits with value on.

For= Example

sequence even bit	even parity bit	odd parity bit
0100010	01000100	01000101
1000000	10000001	10000000

P. T. O

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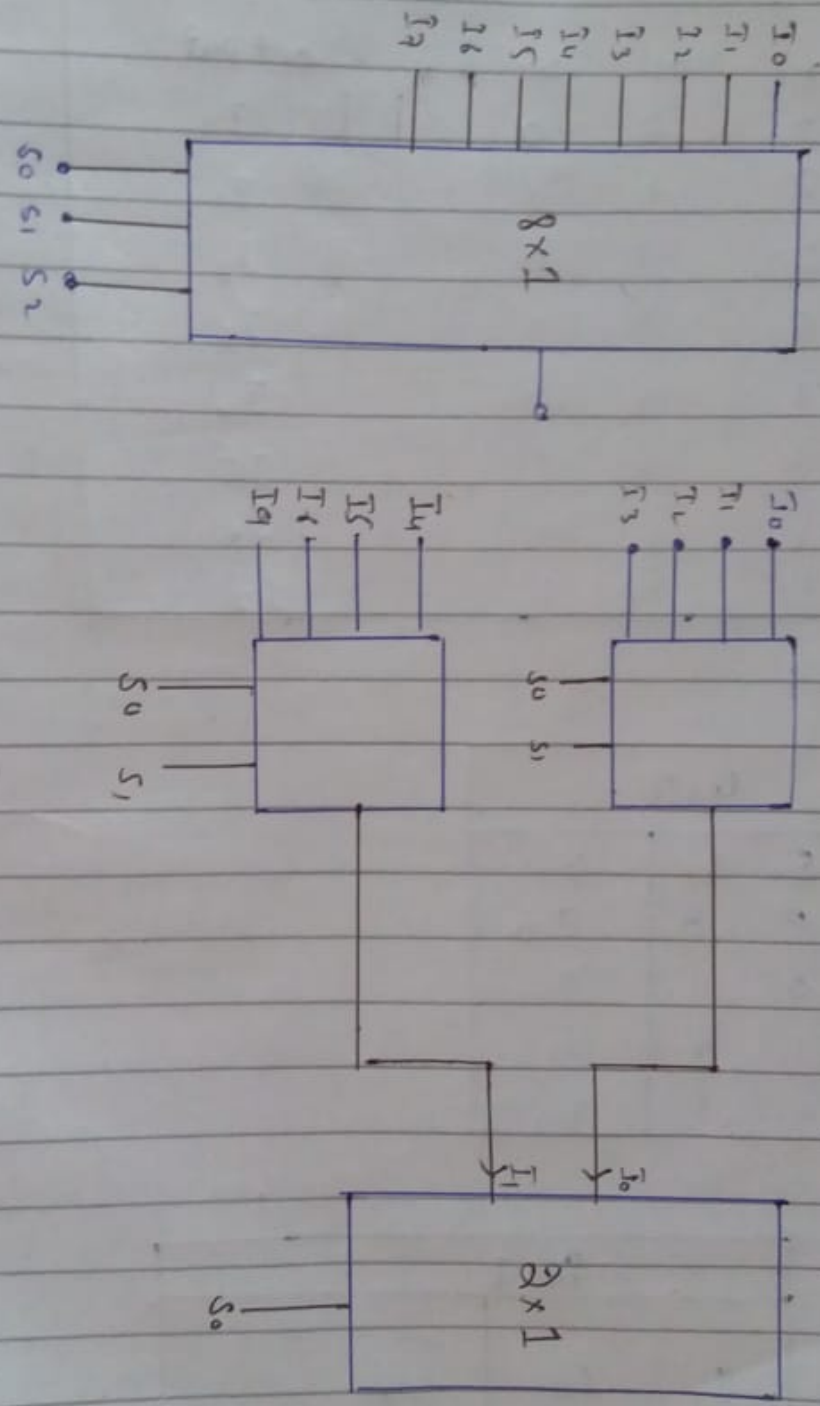
Ans



Q(4).

Ans:- The inverter have always lower limit of the Power depends on the Sum of the NMOS and Vdd.

-> Logic Function is implemented by Pull-down network only

=> Full swing output V_{OL} = Gnd and $V_{OH} = V_{DD}$

=> Faster switching speeds.

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8x1 Mux Truth Table

S_2	S_1	S_0	output
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

4x1

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

2x1

S_1	S_0	Y
0	0	I_0
0	1	I_1

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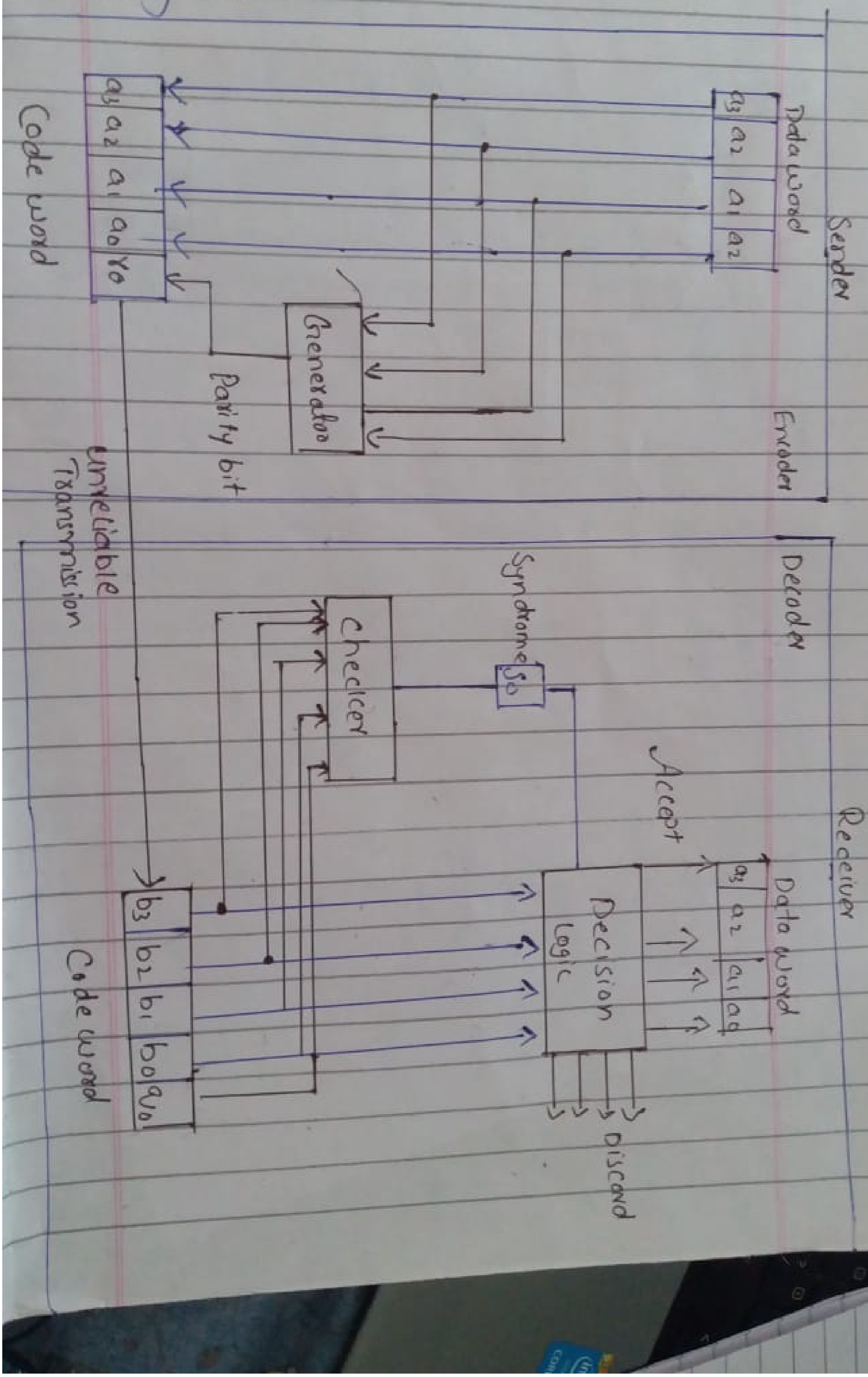
Diagram



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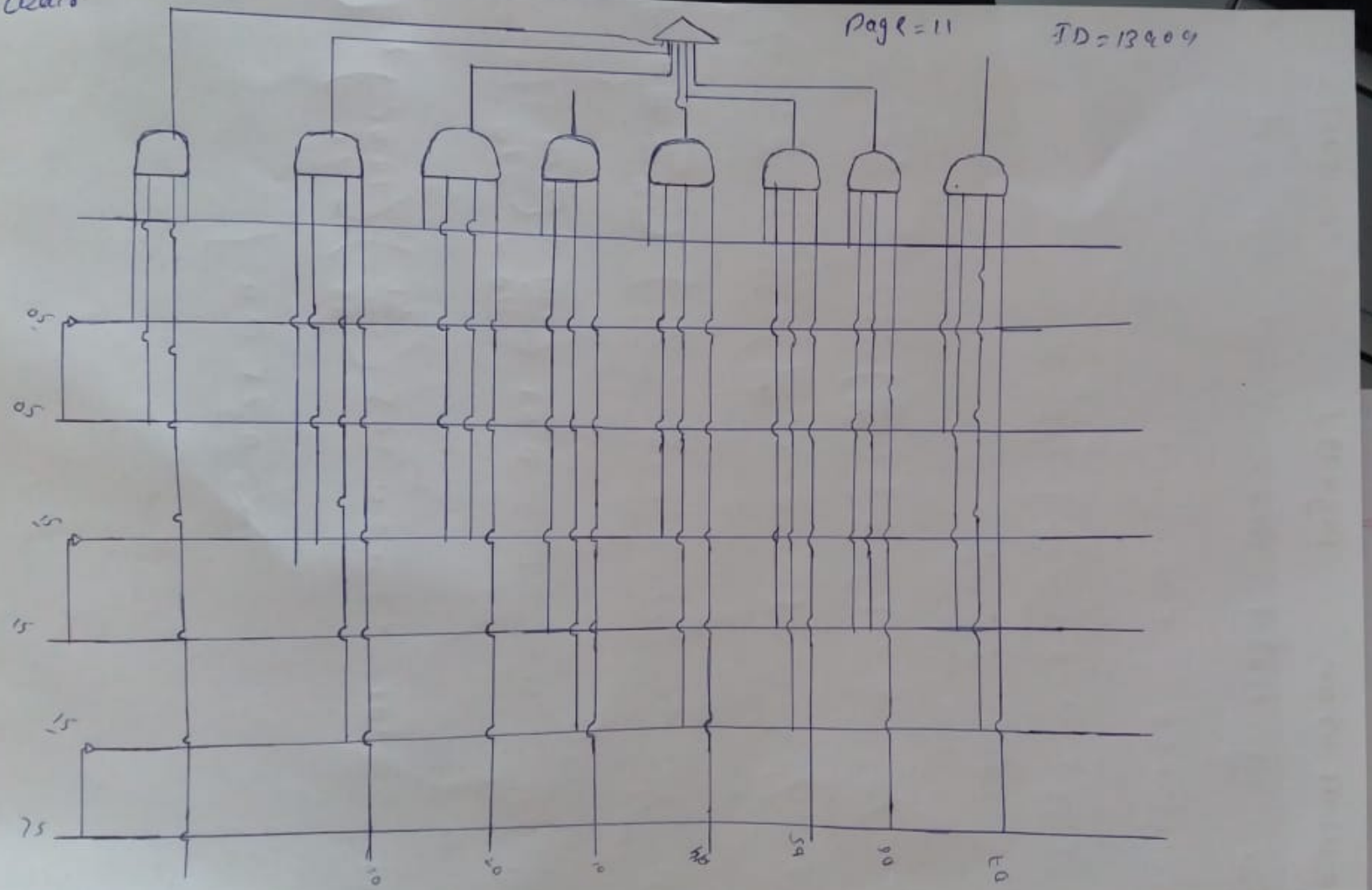

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8x1 mux By VDL method

$I_0 = \bar{S}_2 \bar{S}_1 \bar{S}_0$

$I_1 = \bar{S}_2 \bar{S}_1 S_0$

$I_2 = \bar{S}_2 S_1 \bar{S}_0$

$I_3 = \bar{S}_2 S_1 S_0$

$I_4 = S_2 \bar{S}_1 \bar{S}_0$

$I_5 = S_2 \bar{S}_1 S_0$

$I_6 = S_2 S_1 \bar{S}_0$

$I_7 = S_2 S_1 S_0$