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PAPER : DIGITAL LOGIC DESIGN.
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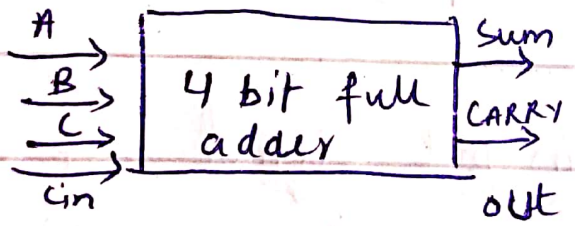
Q:1) Draw and explain logic diagram for each of following.

(A) A circuit for adding or subtracting two 4-bit number :-

(1) 4-bit full Adder:

The full adder is logical circuit, that perform an addition operation on three binary digits and just like an half adder, it also generate carry. In many ways full adder can be used as half adders connected together.

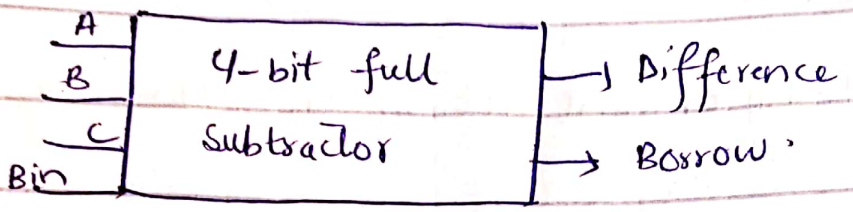


Cin
A
B
C
Sum

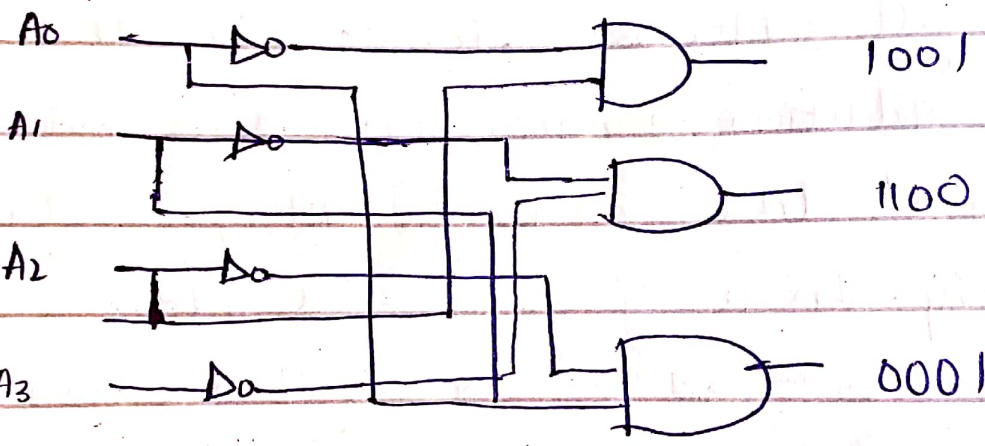
(b) 4-bit full Subtractor:

The 4 bit full subtractor is logical circuit & that perform subtraction operation on three binary digits, & just like on half subtractor, it also generate Borrow. In may ways full

Subtractor can be used as half subtractor connected together.

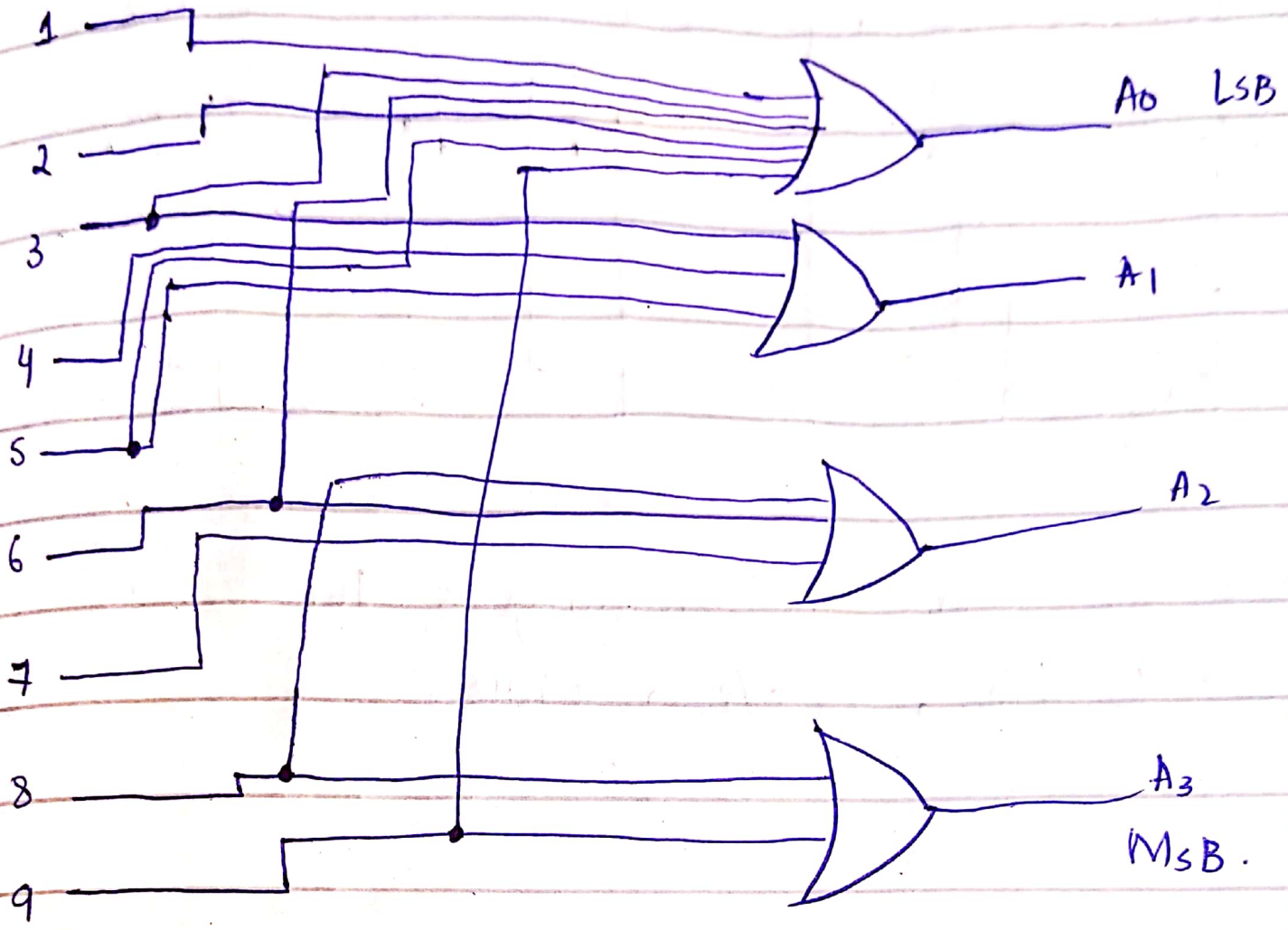


(b) 4-bit active Low Decoder:



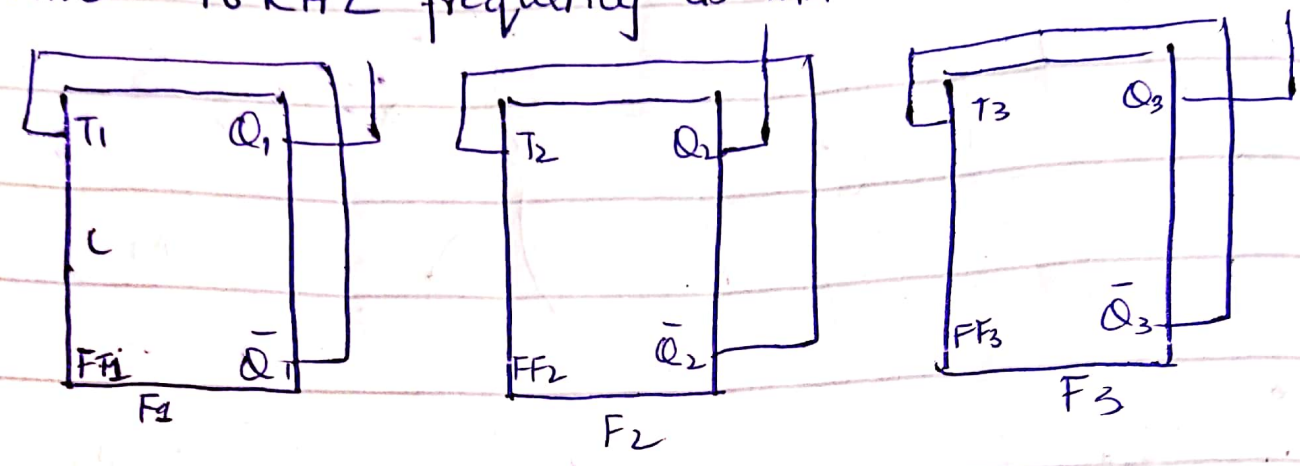
Here we use 4 bit input signal A & it detects the value 1001. The active low decoder means that output is active, it has logic value, which is low, rather than logic value high. This decoder works as active low enable input is high.

(c) DECIMAL TO BCD ENCODER :-



A decimal to BCD encoder is also known as 10 line to 4-line encoder it accepts 10 inputs and product 4-bits output corresponding to activated decimal input.

(9) Frequency divider (use 3J-K flip flop and assume 16 KHZ frequency as initial waveform).



Here we assume the frequency is 16KHZ

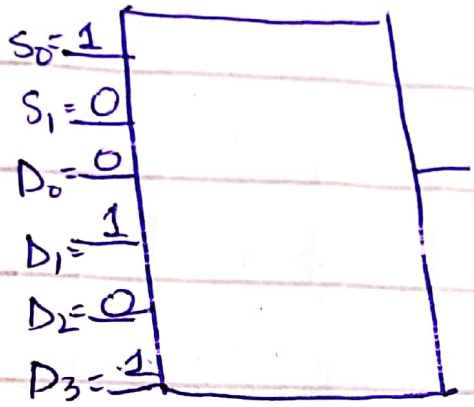
So $f/2$, $f = 16/2 \Rightarrow 8$ KHZ.

Q:2 : For 4 input multiplexer, data inputs are given as

$D=0$, $D_1=1$, $D_2=0$, $D_3=1$.

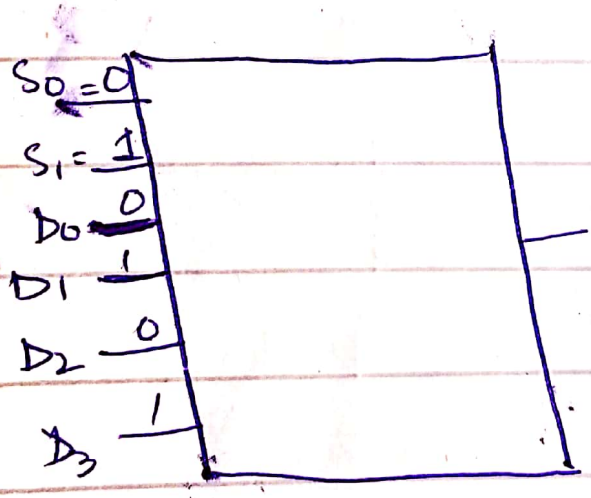
find input x if select input are.

(a) $S_0=1$, $S_1=0$



$S0 . S1 = 10 . D①$

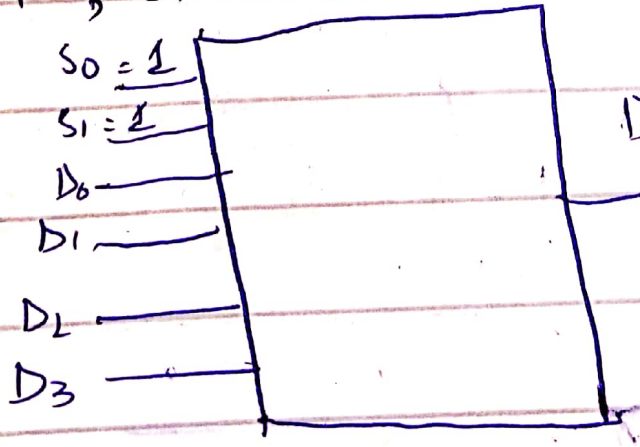
(b) $S0=0$, $S1=1$.



$S_0 . S_1 = D1$

0 : 1

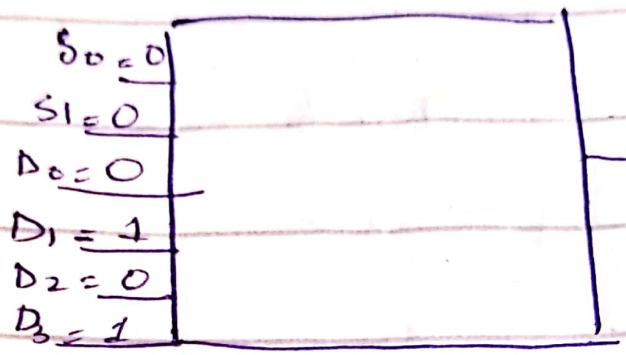
(c) $S0=1$, $S1=1$



$S0 . S1 = D2$

1 . 0

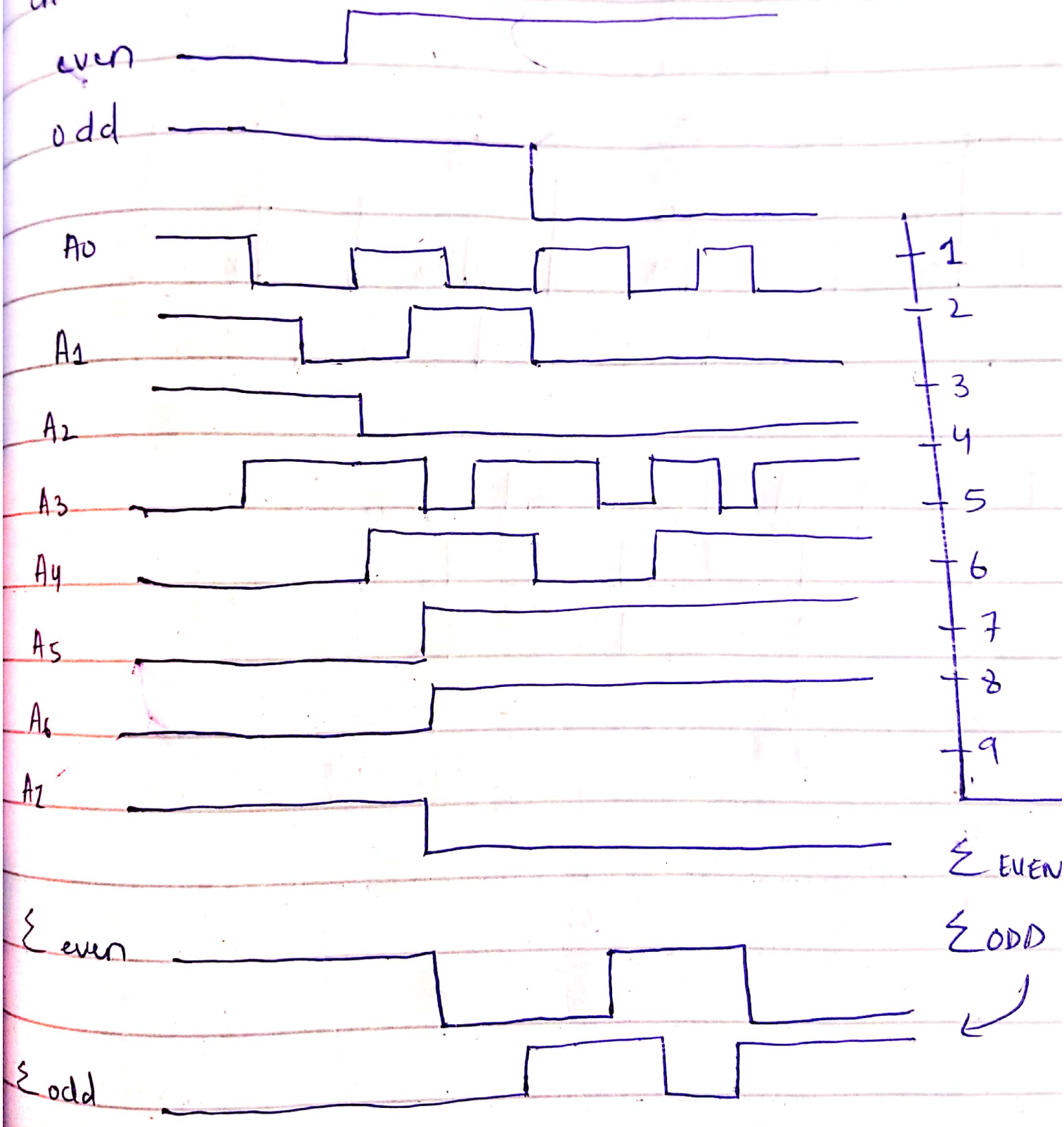
(d) $S_0 = 0$, $S_1 = 0$



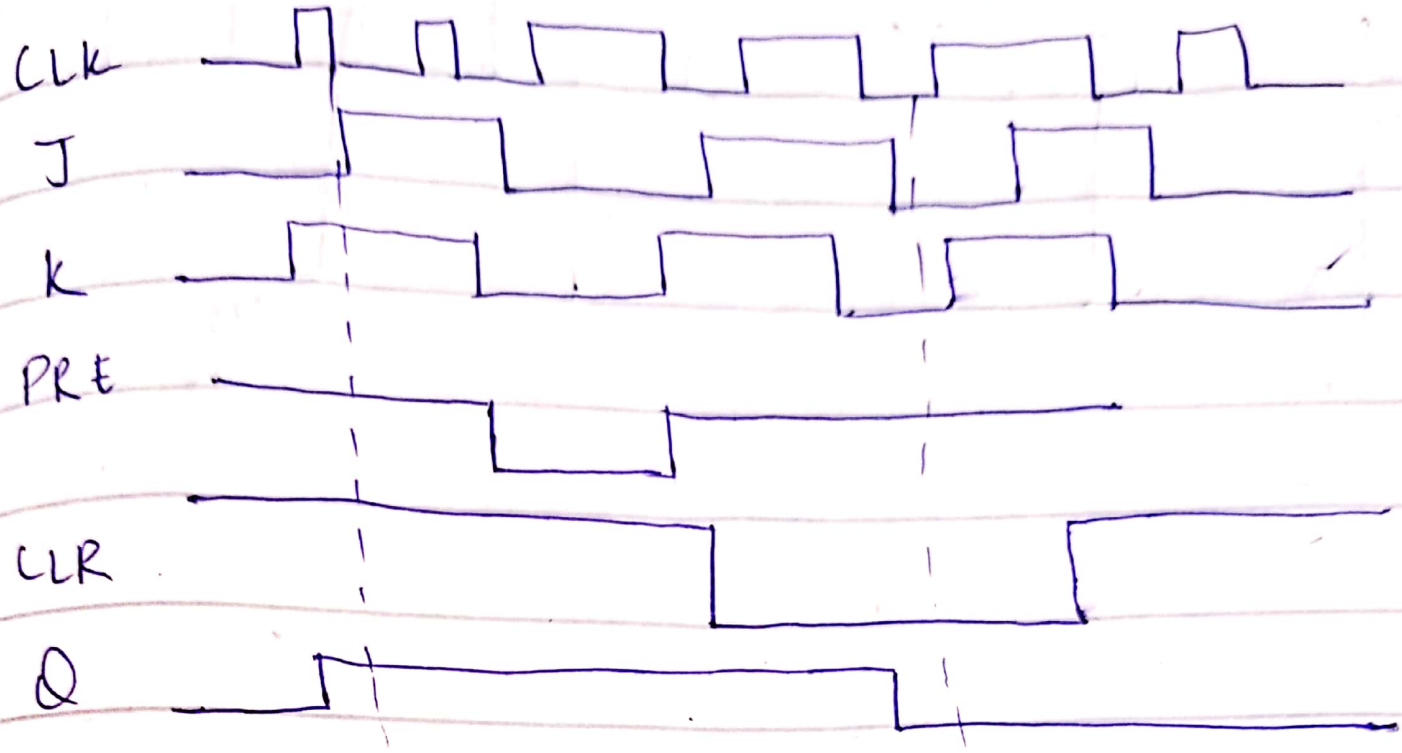
$S_0 . S_1 = D_3$

1 . 1 .

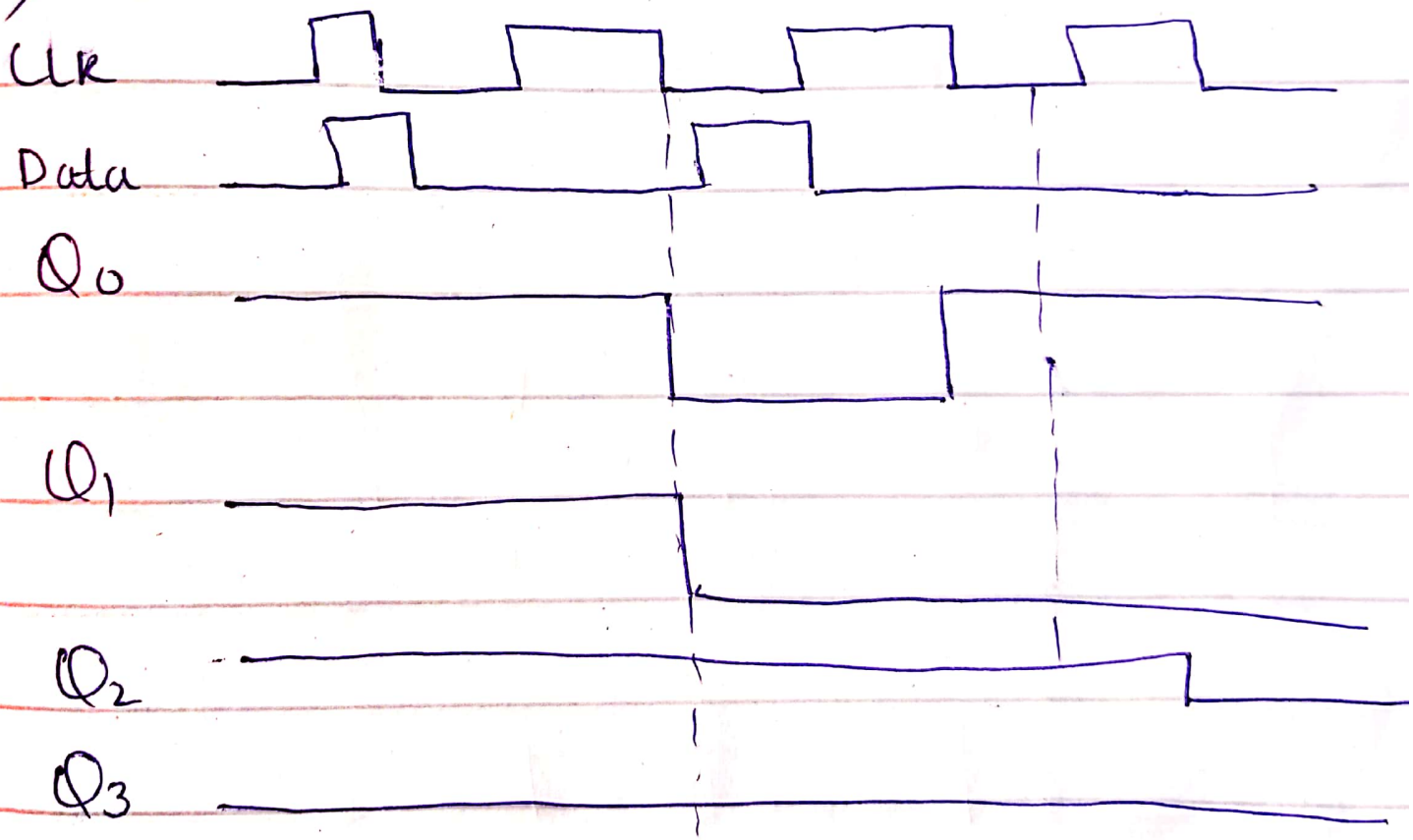
Q:3 Timing diagram in figure: 01 shows inputs to a 9-bit parity checker. Draw the Σ even and Σ odd, output for every parity checker.

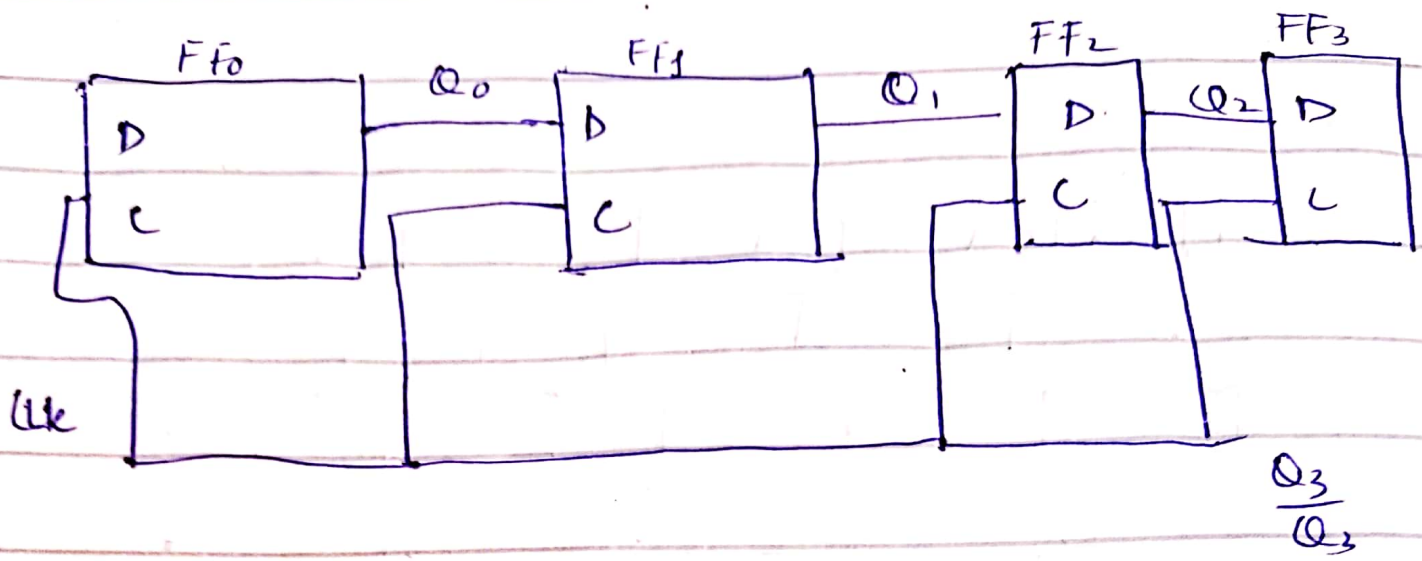


Q4



Q:5)





Question : 6

Draw the logic diagram and timing diagram for the 4-stage synchronous binary counter. Verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.