Digital Logic Design

Assignment: 6

Sir. Muhammad Amin.

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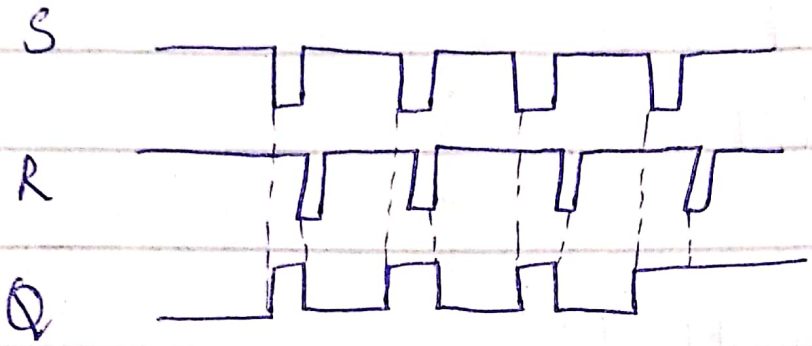
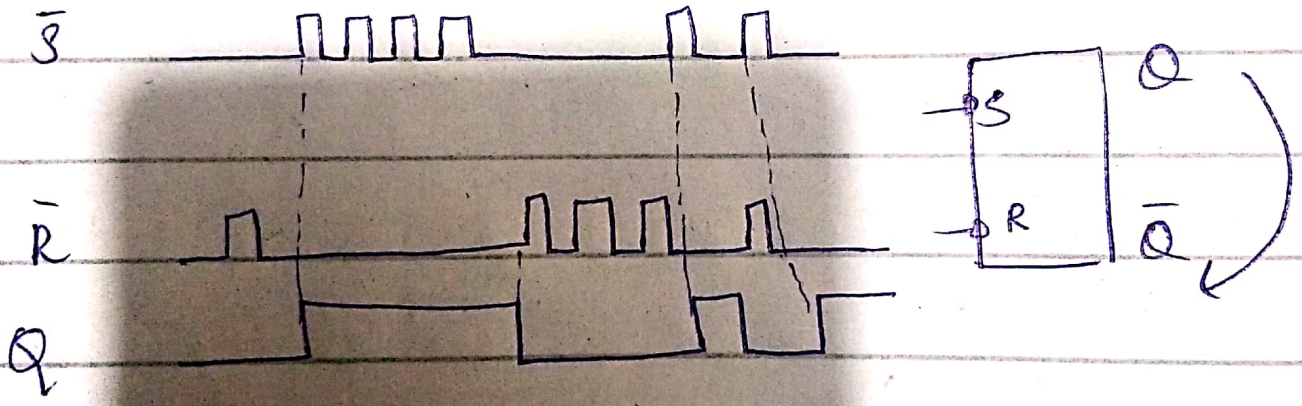
Department: Cs.

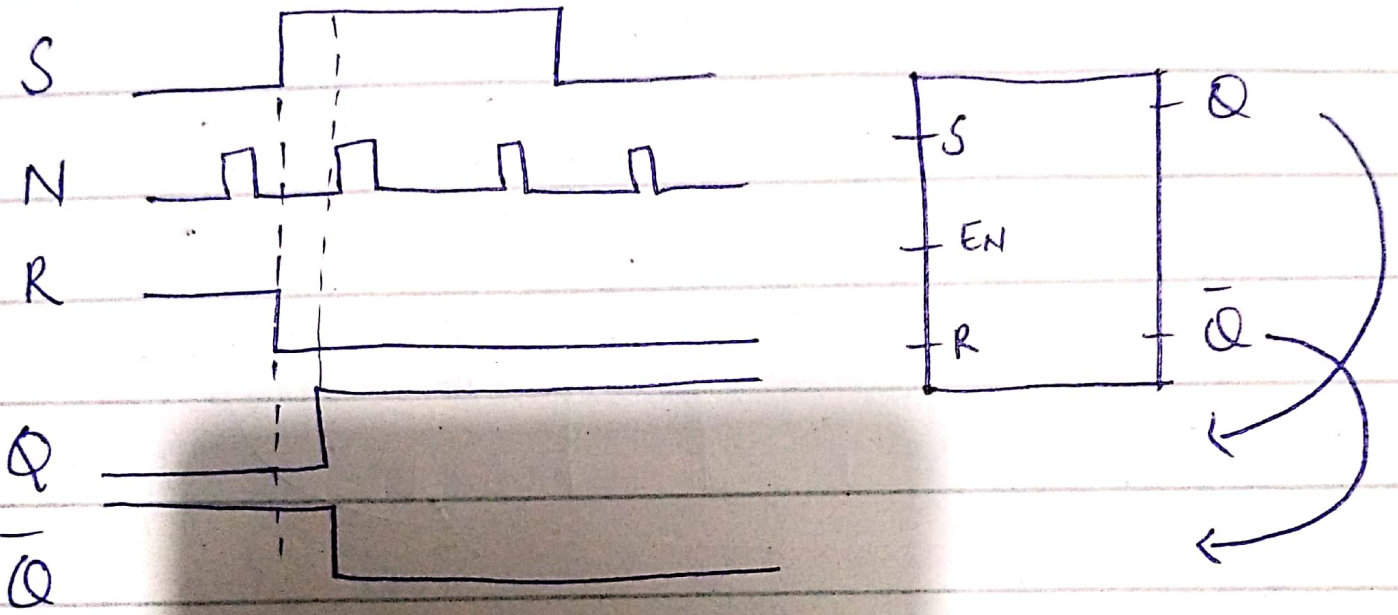
Q : 1 .



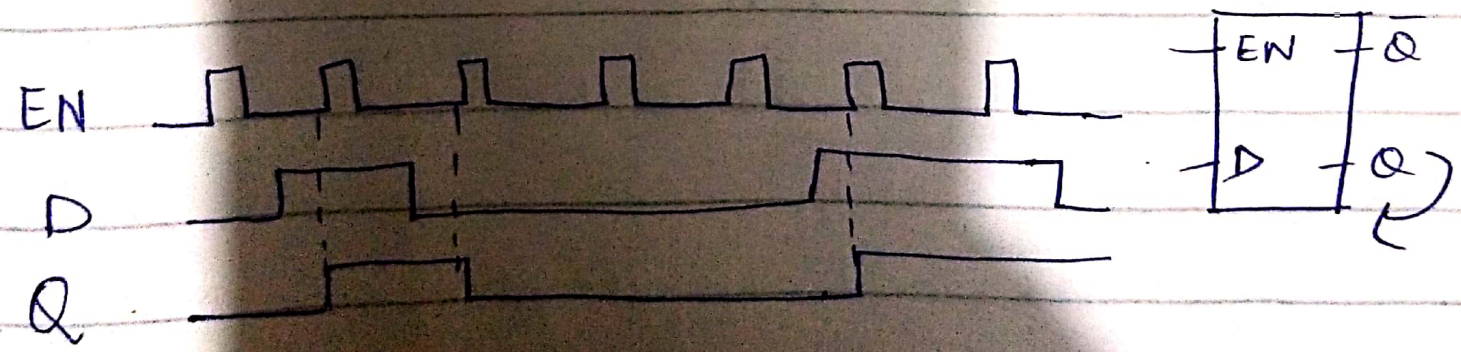
Q : 2



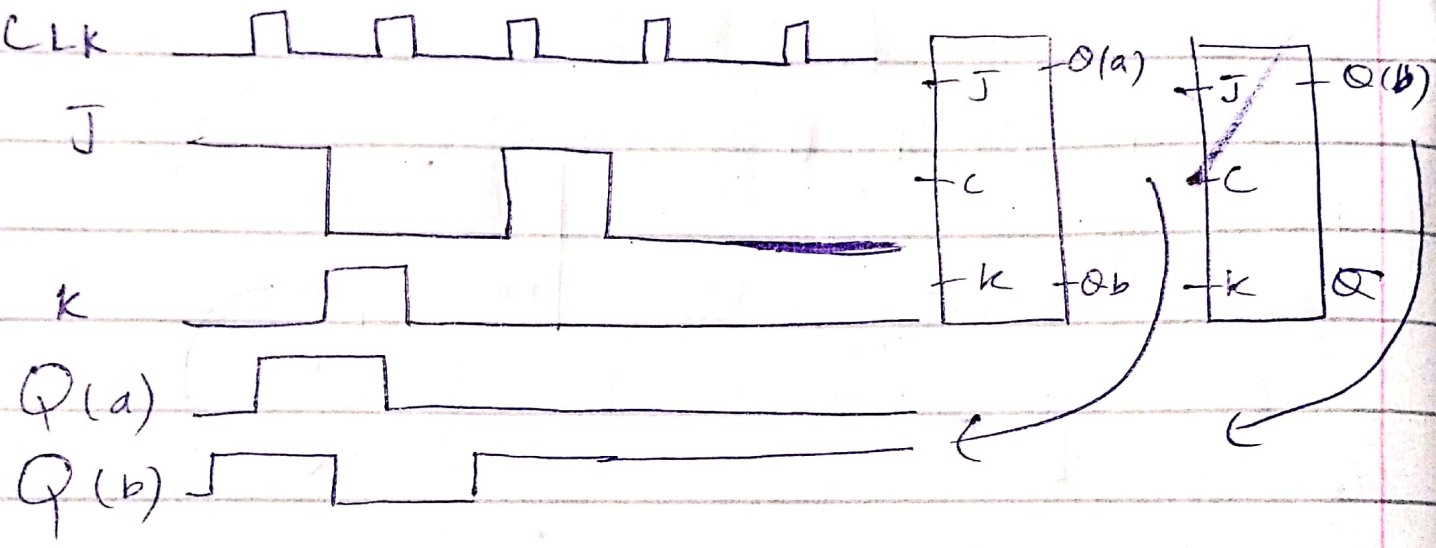
Q:3)



Q:4)



Q:5:

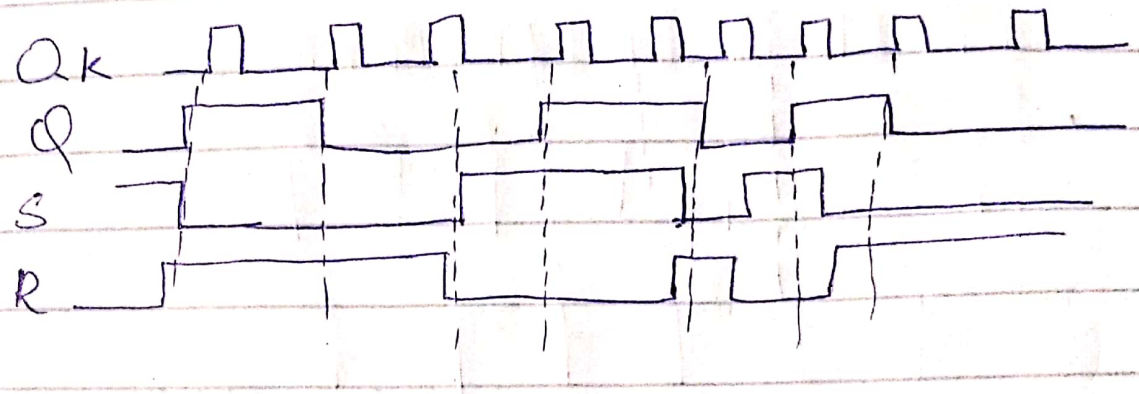


The main difference between (a) and (b) edge triggered JK-flip-flops is that

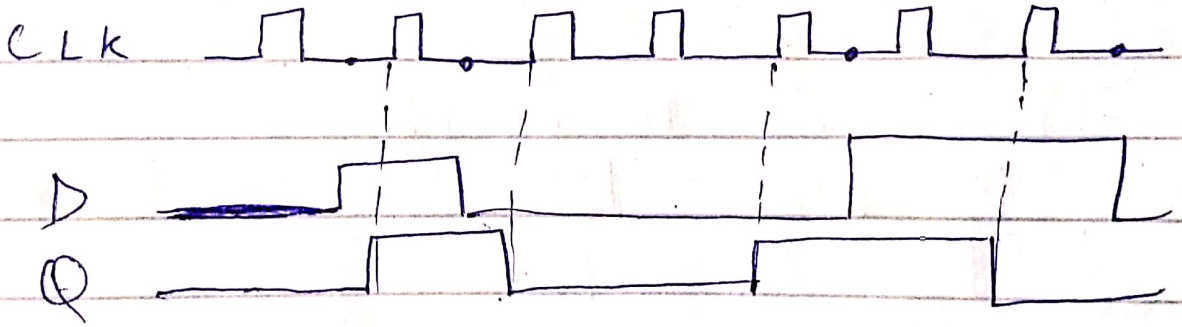
"The flip flop (a) on the negative edge of the clock pulse, while.

The flip-flop (b) triggers on the positive edge of the clock pulse

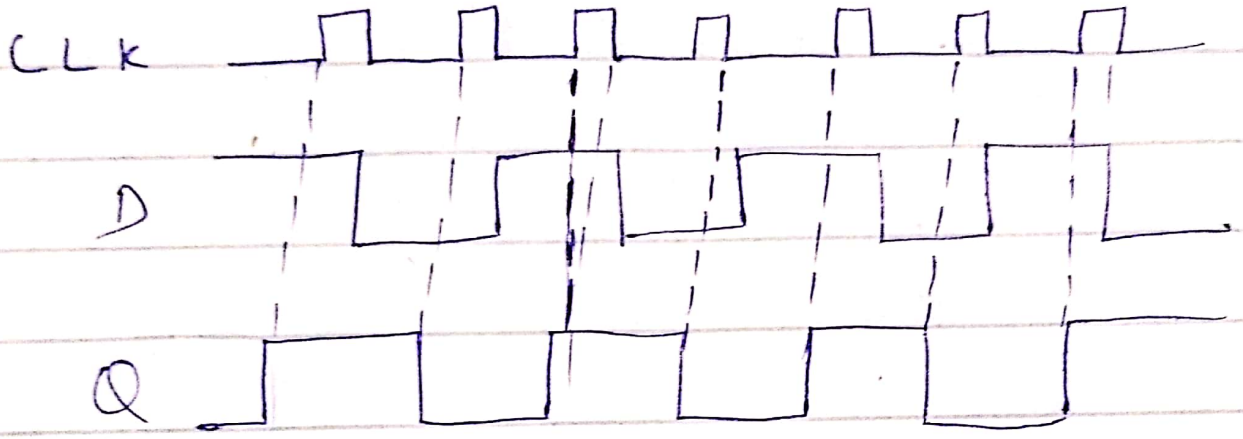
(6)



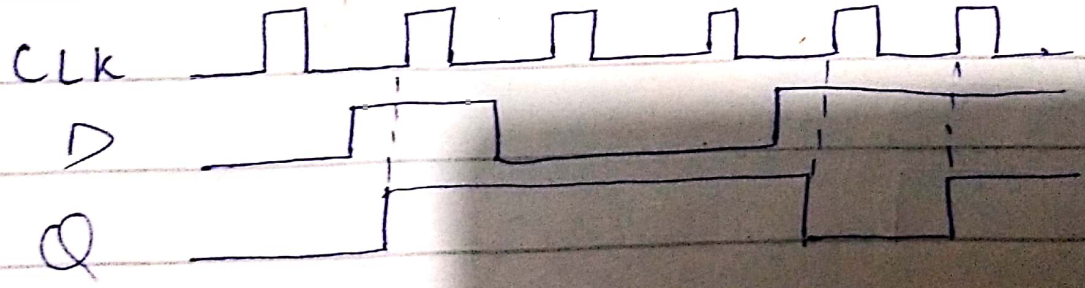
Q: 7.



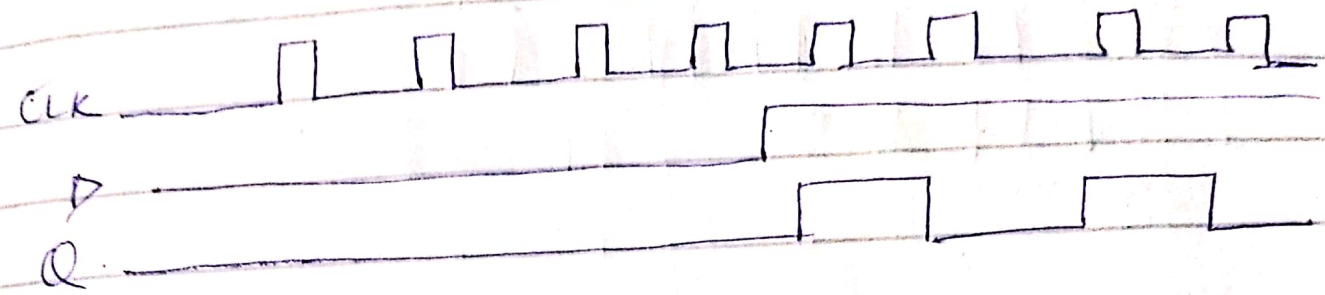
Q : 8 :-



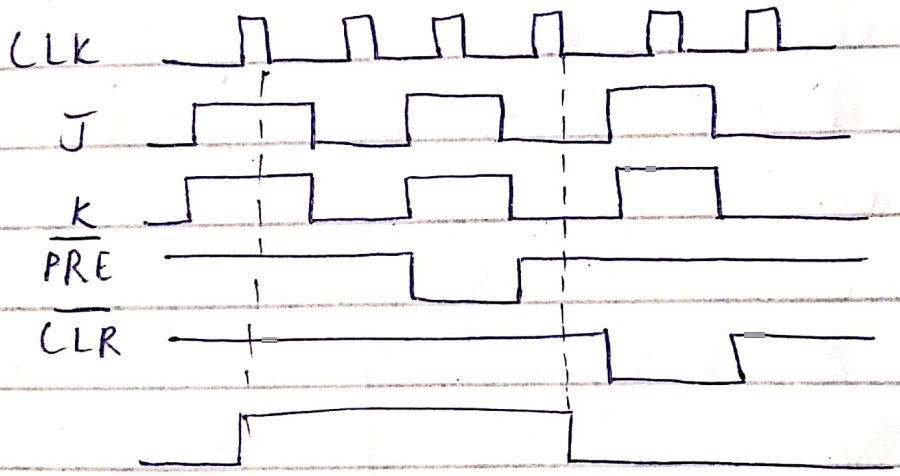
Q : 9)



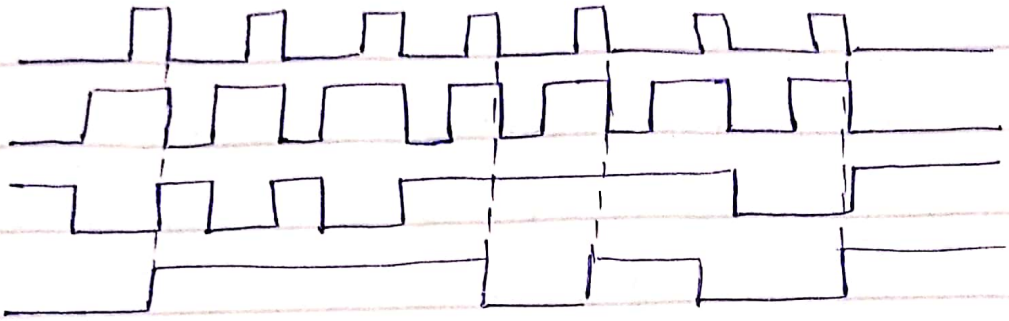
Q: 10:



Q: 11:



Q : 12 :



Q : 13)

$J_1 = 1010011$.

$J_2 = 0111010$

$J_3 = 1111000$

$J = 0010000$

$k_1 = 0001110$

$k_2 = 1101100$

$k_3 = 1010101$.

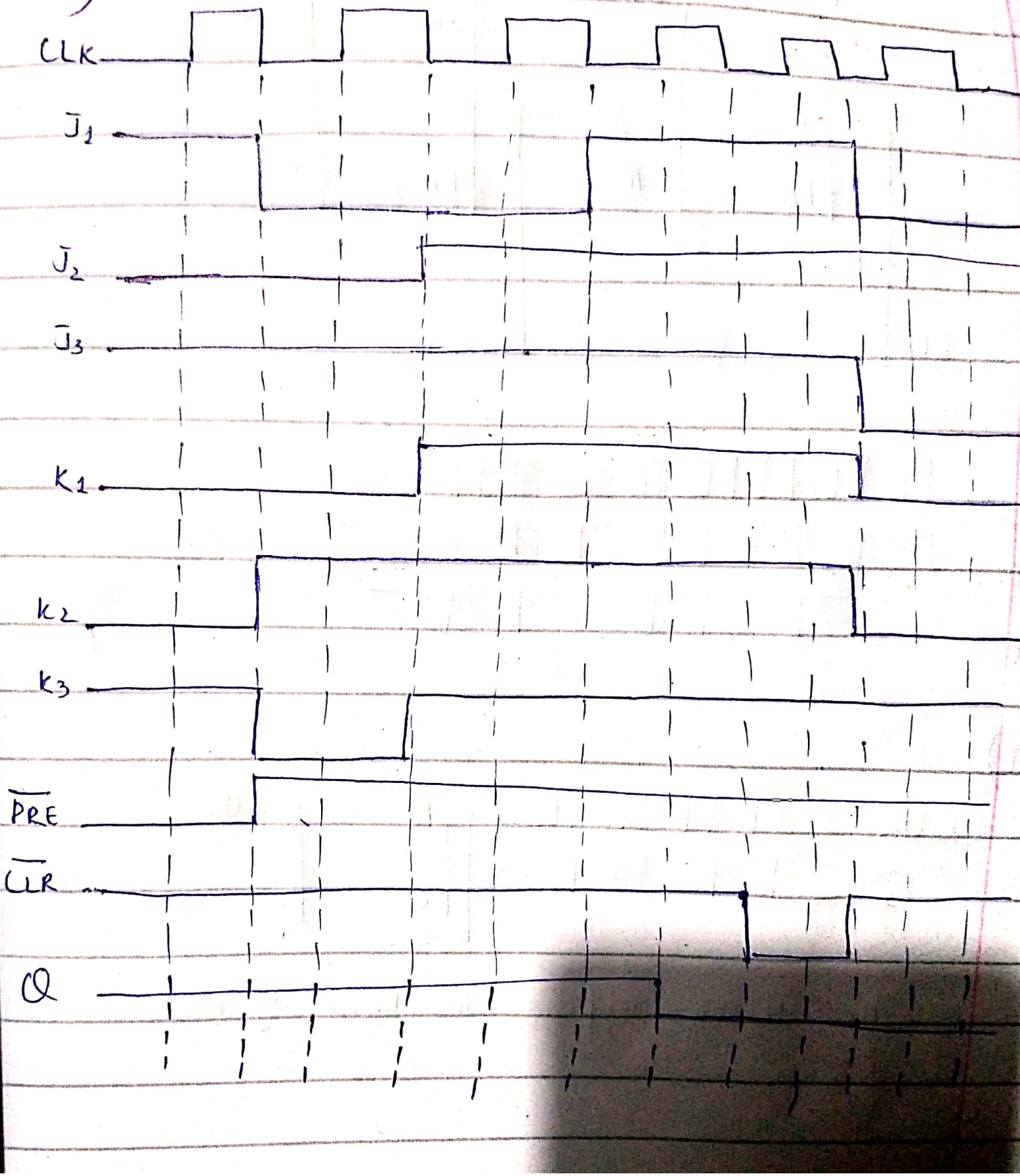
$k = 0000100$.

$J = 0010000$

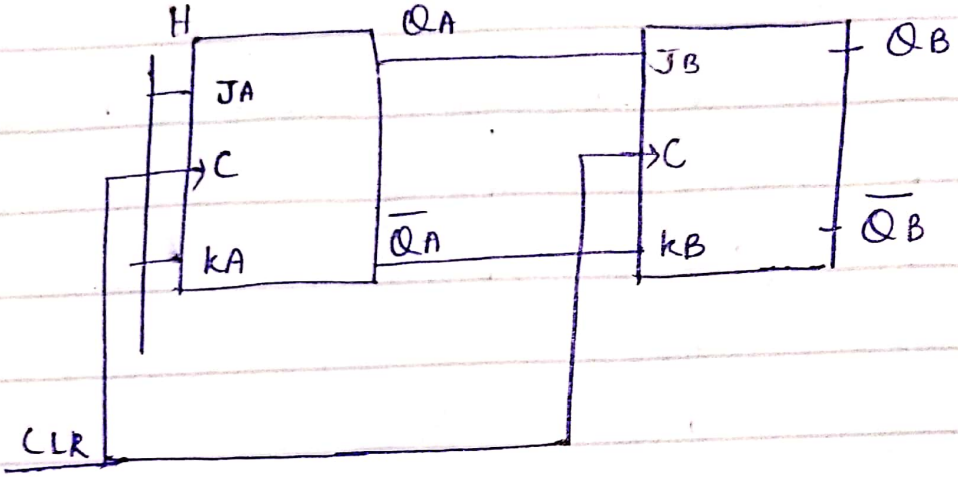
$k = 0000100$.

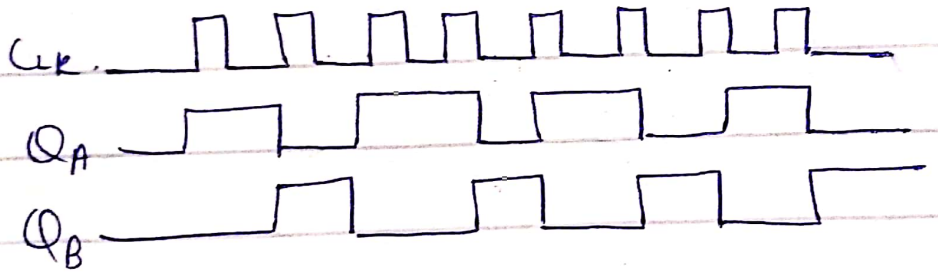
$Q = 0011000$.

Q:15)

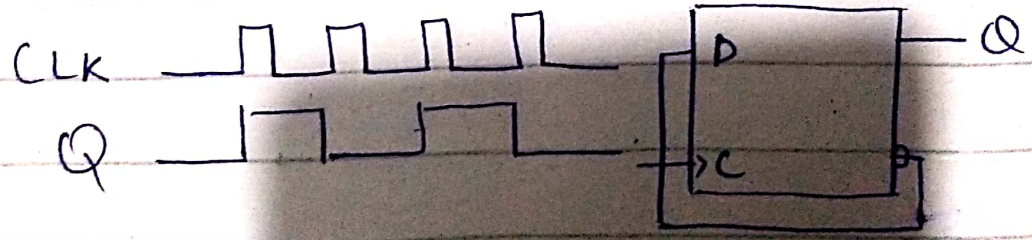


Q: 16)



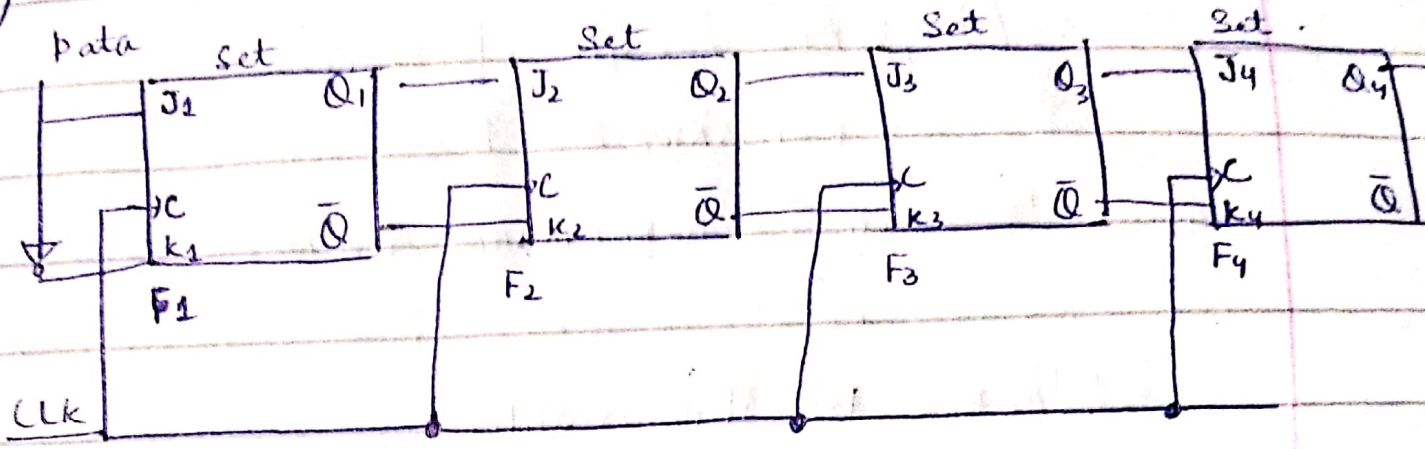


Q: 17).

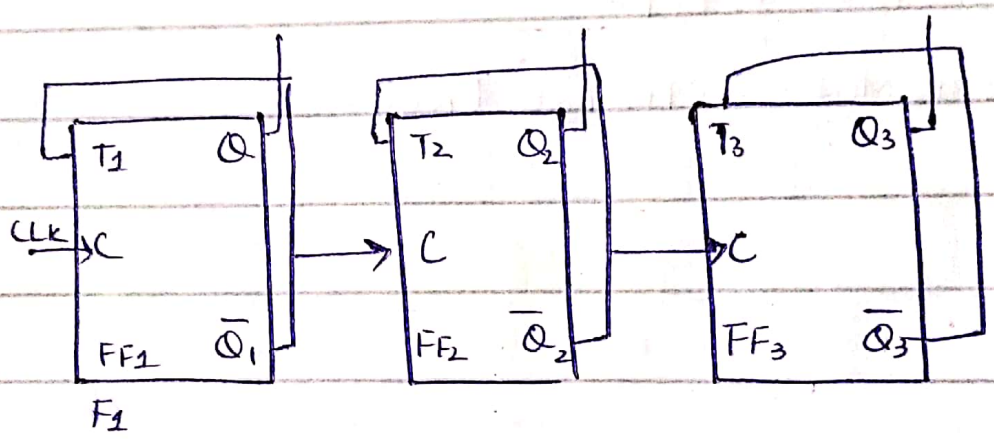


The device performs the Divide-by-two function.

Q: 18)



Q: 19)



Here if the input frequency is 8KH then at given modes frequency will be as follows.

$Q_A = 8/2 = 4kh.$

$Q_B = f/4 = 2kh.$

$Q_C = f/8 = 1kh.$