Name : Irfan ullah

ID : 15431

Assignment : no 6

Subject : Digital Logic Design

Course code(CS) : CSC-201

Program : BC (CS)

Assignment No. 6

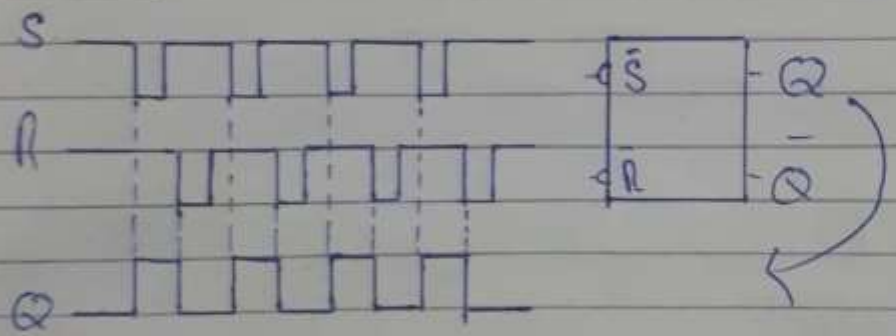
Name : Irfan ullah

ID : 15431

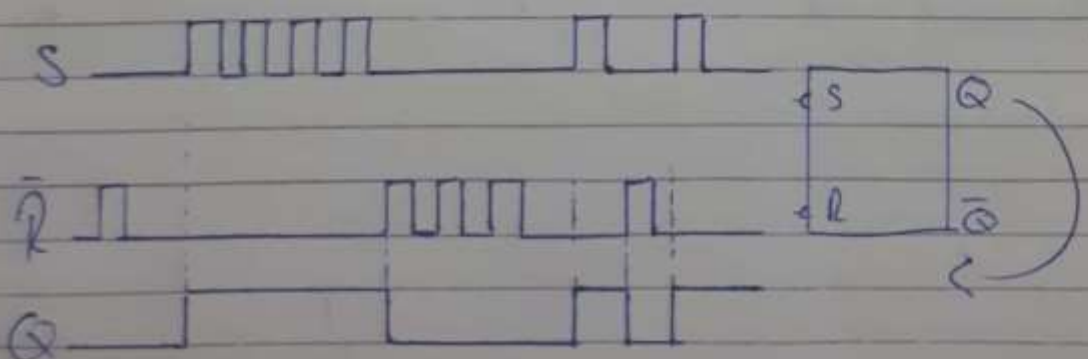
Subject : DLD

Program : BC(CS)

Q1



Q2



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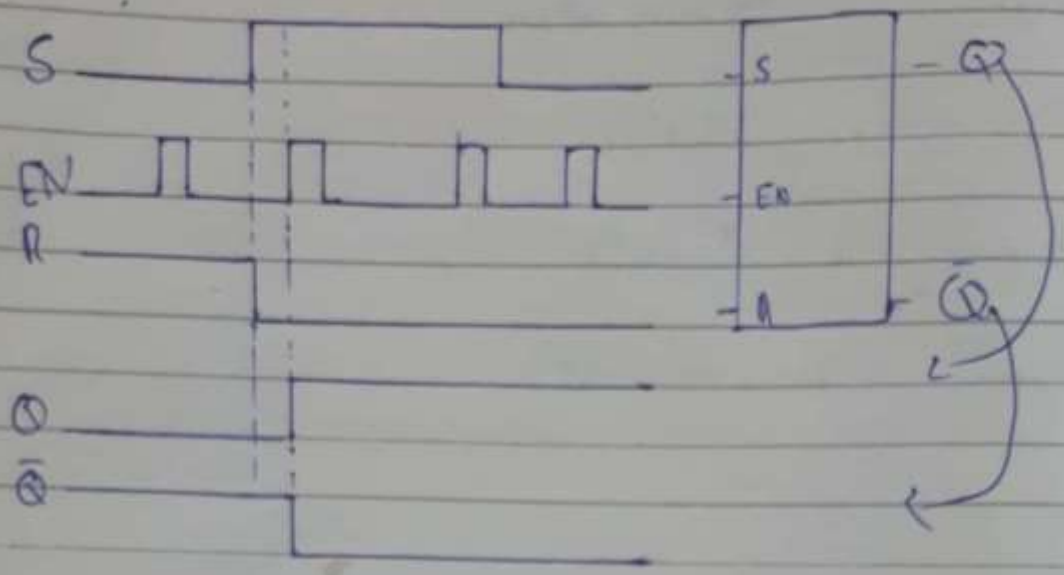

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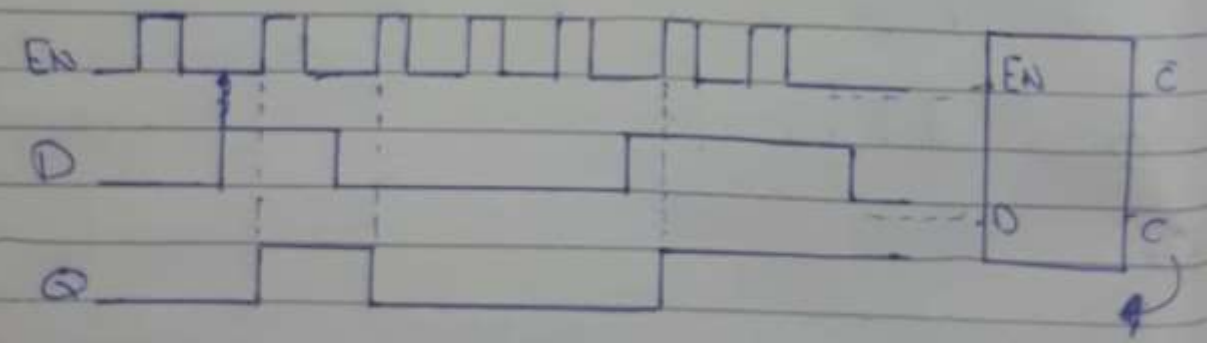

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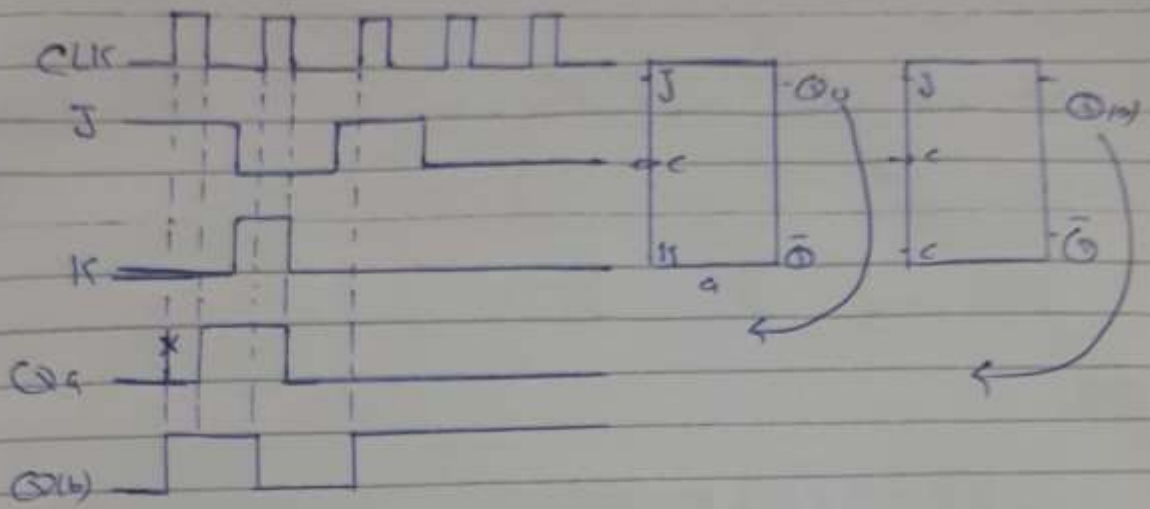
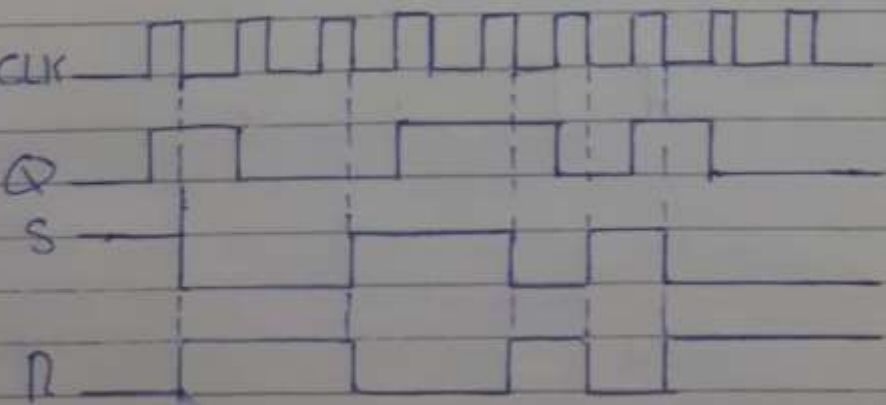


The main difference between (a) and (b) edge triggered JK-flip-flops is that

The Flip Flop (a) on the Negative edge of the clock Pulse while

The Flip Flop (b) triggers on the + Positive dge of the Clock Pulse.

(6):-



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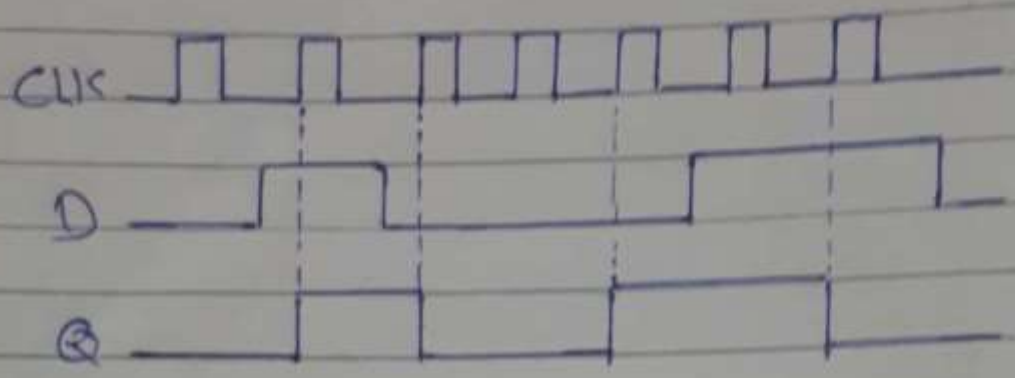

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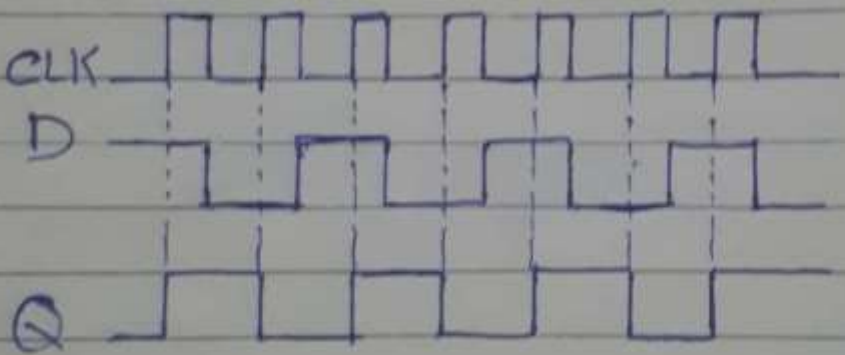

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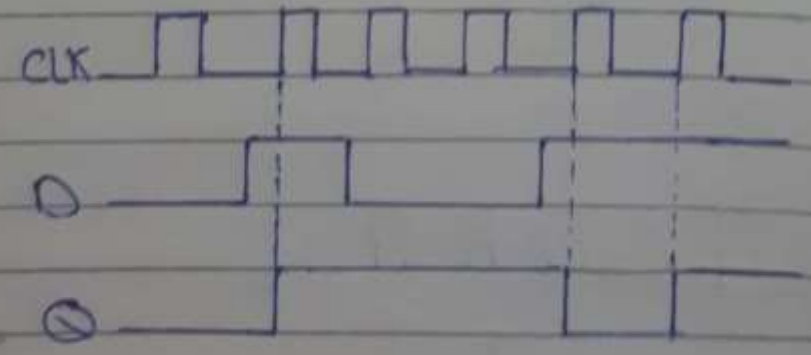

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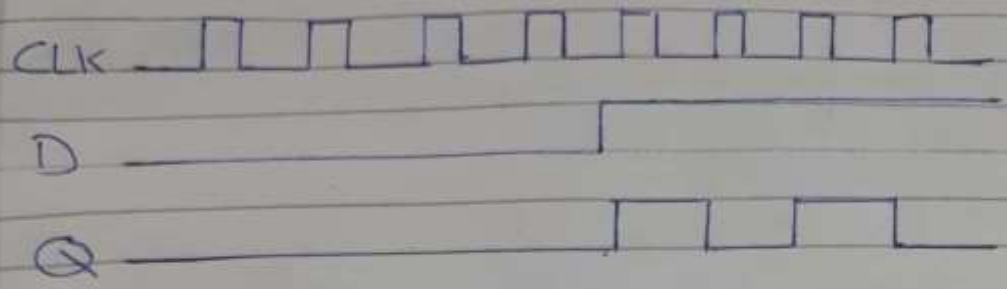

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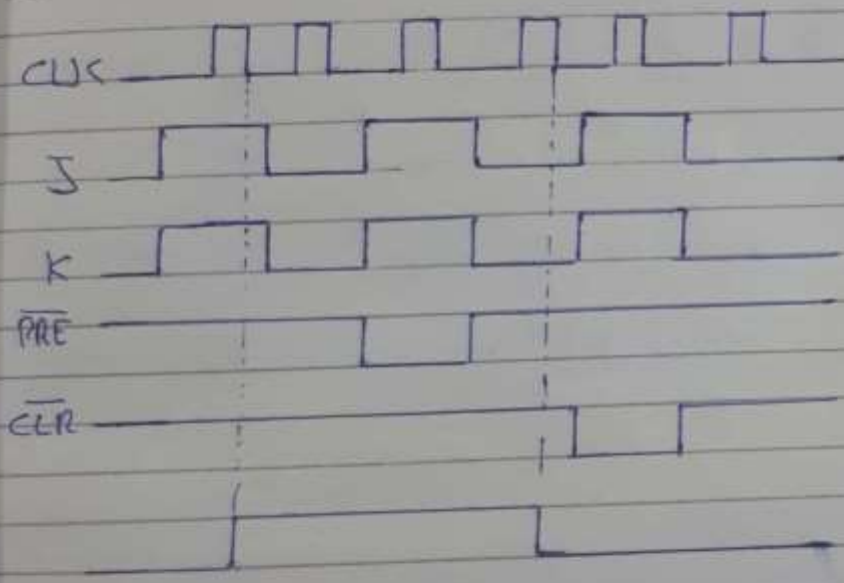

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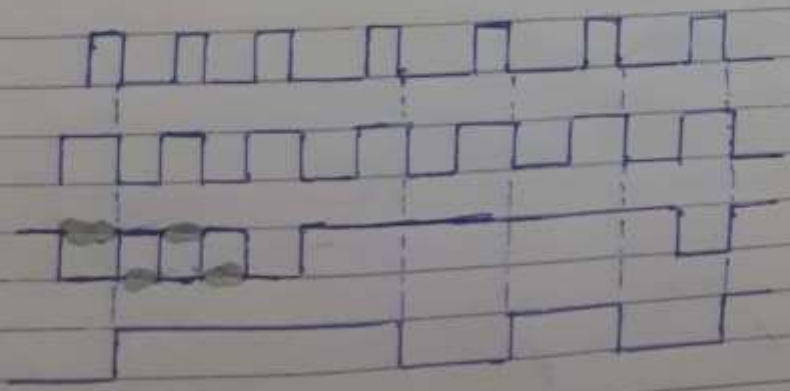


Q13.:

$J_0 = 10100011$

$J_1 = 01110110$

$J_2 = 11110000$

$J = 00100000$

$K_1 = 00011110$

$K_2 = 11011000$

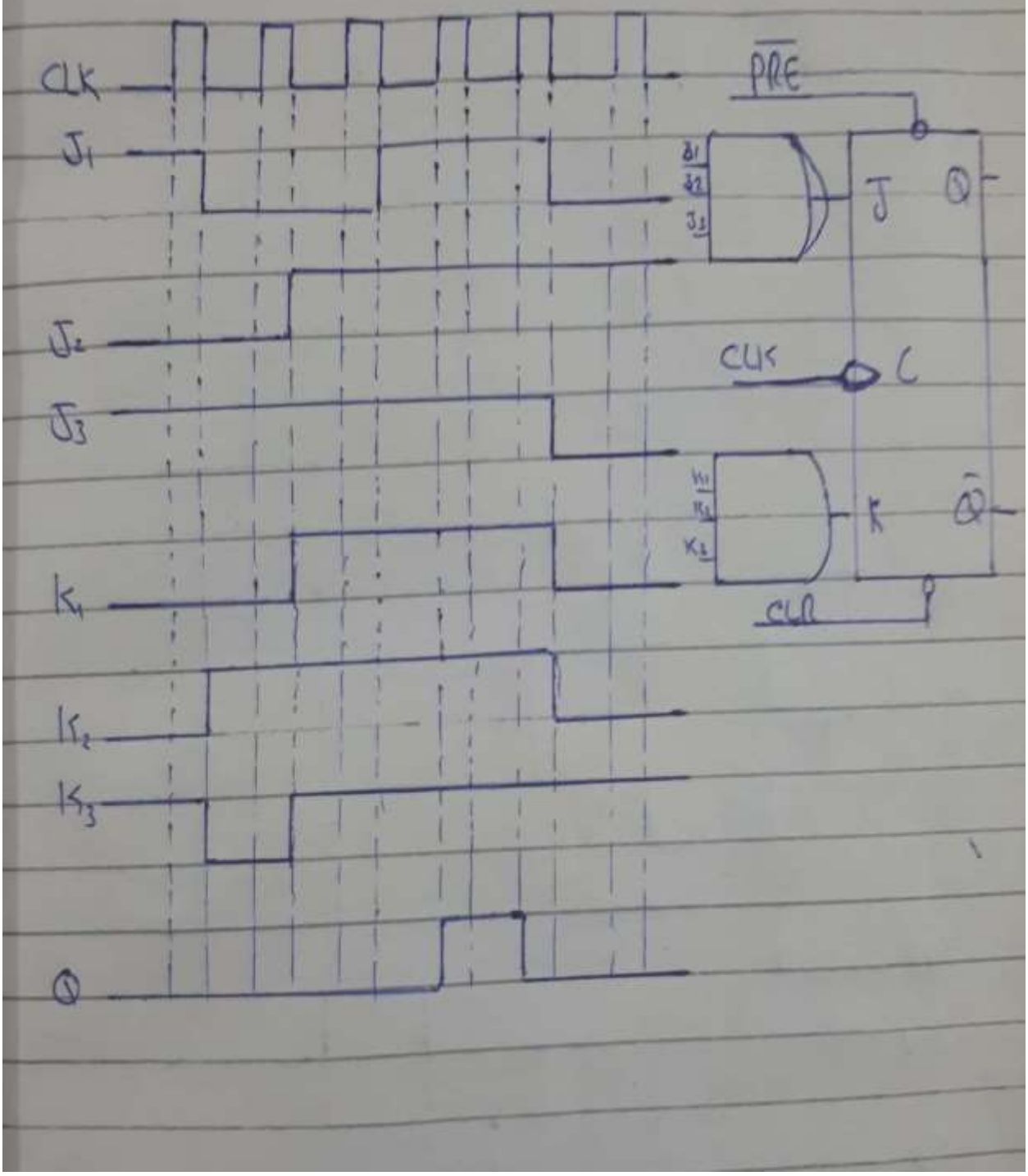
$K_3 = 00000100$

$J = 00100000$

$K = 00000100$

$Q = 00110000$

D14:-



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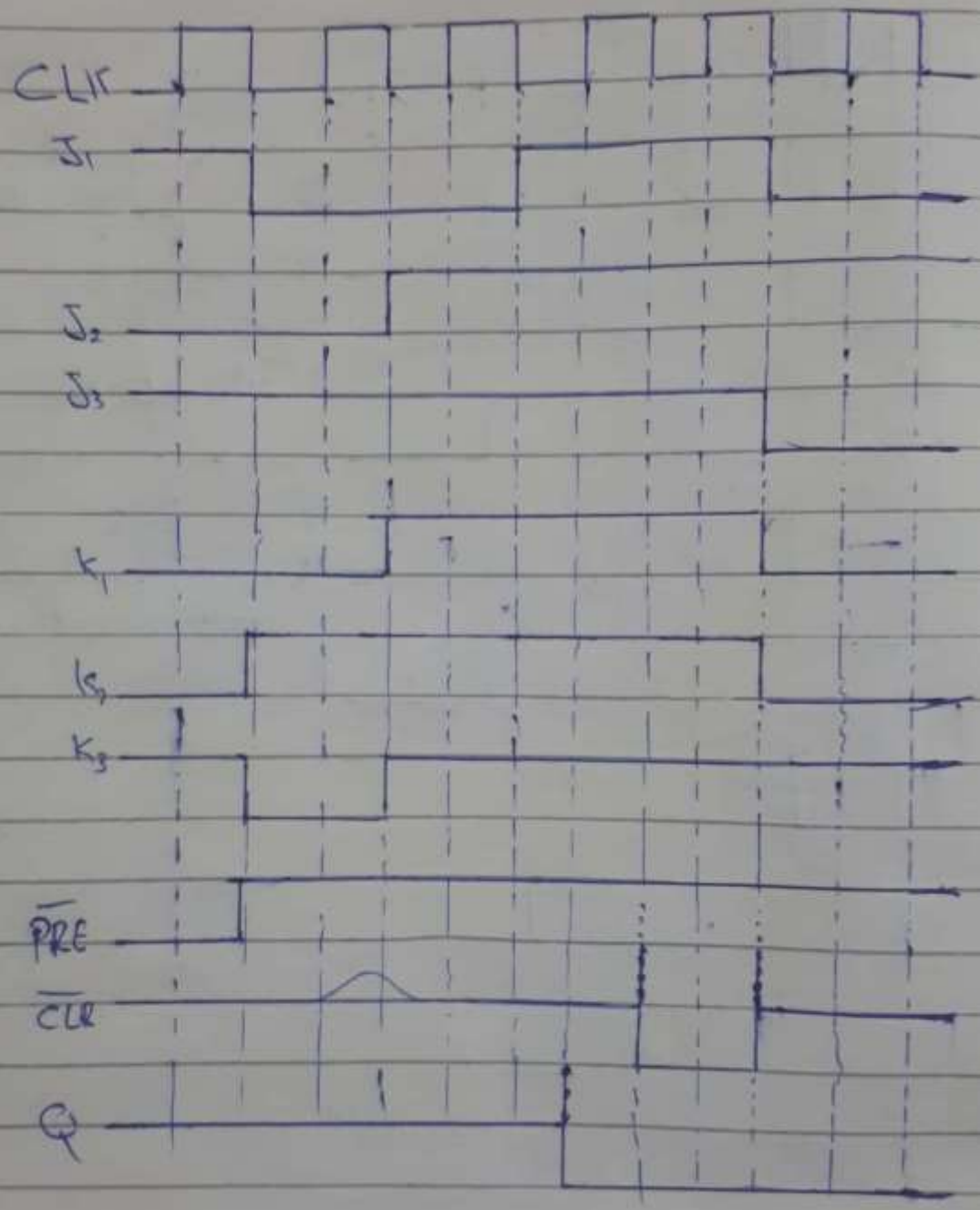

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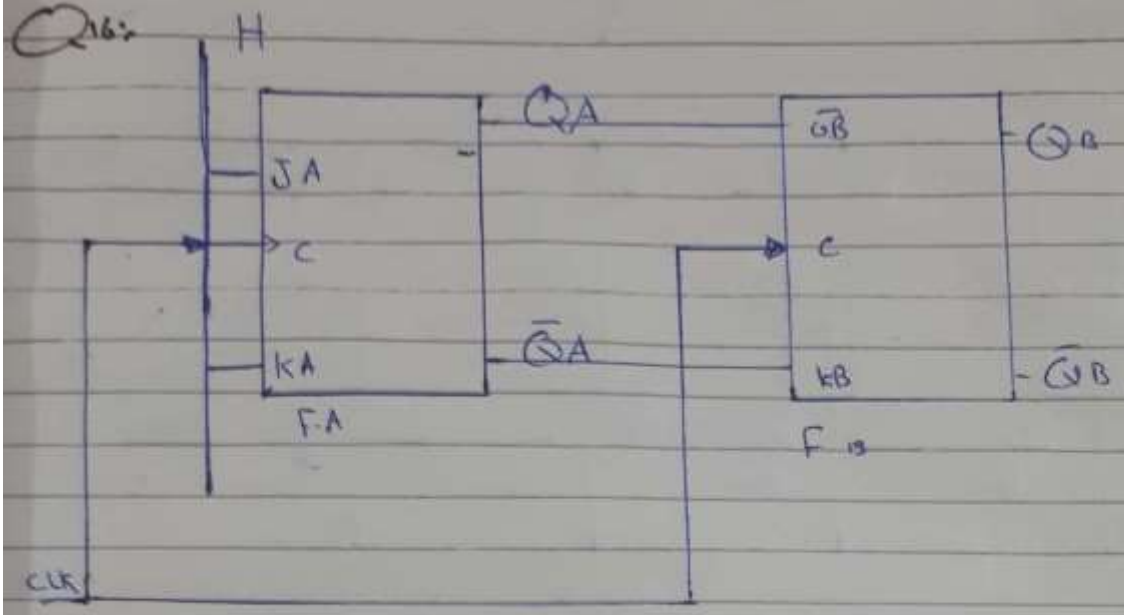

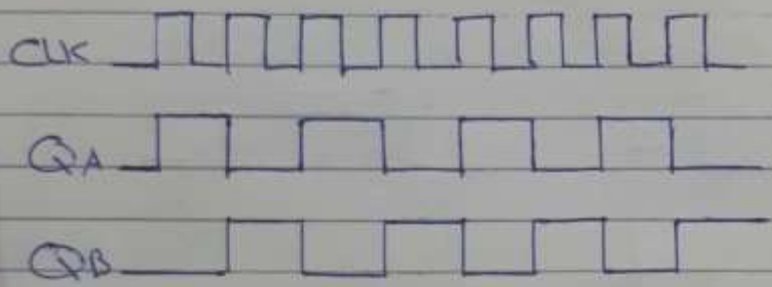

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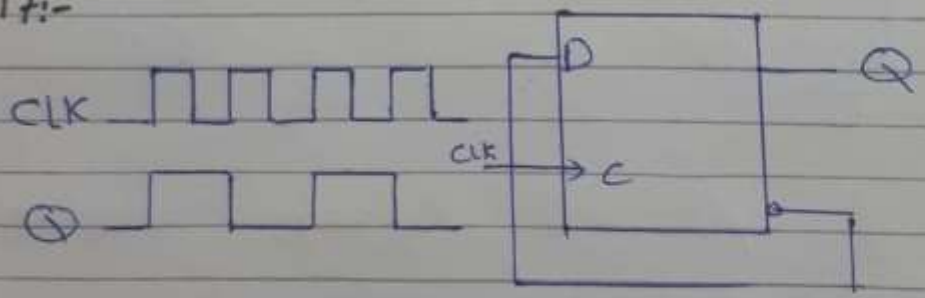
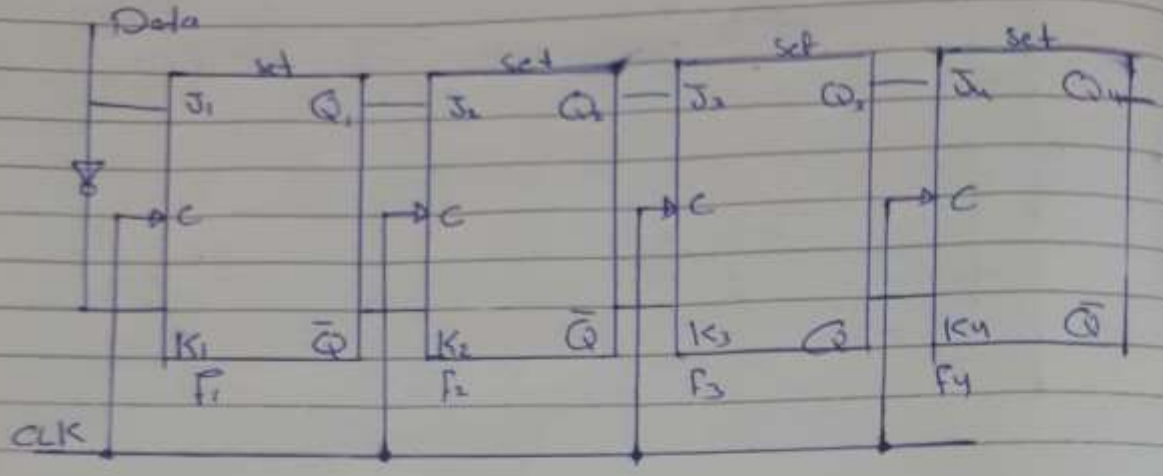


The device Performs the Divide-by-two function

Q18:-



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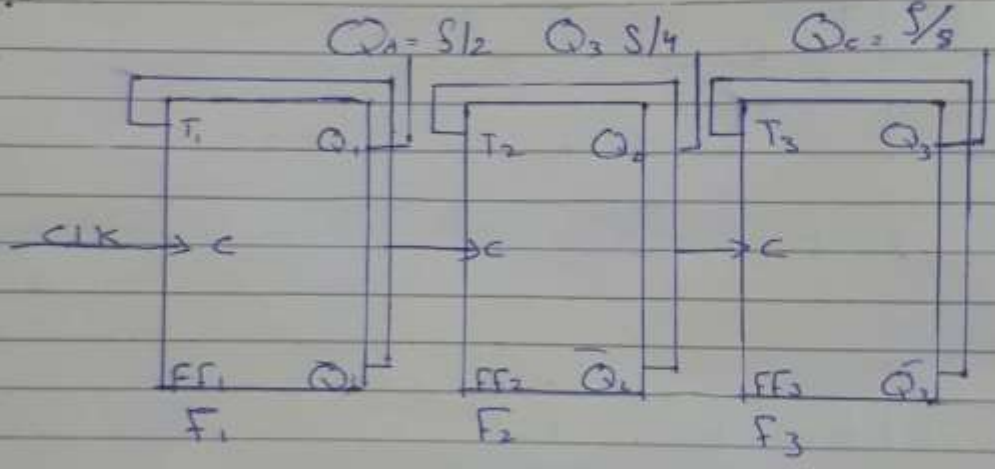

Here if the input frequency is 8kH then and given marks frequency will be as follows

$Q_A = 8/2 = 4kh$

$Q_B = 8/4 = 2kh$

$Q_C = 8/8 = 1kh$