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Assignment 5

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Q1:- Determine the output of a full-adder for the following input A=1, B=0, Cin=1

Ans:-

$\Sigma = (A \oplus B) \oplus C$

$\Sigma = (1 \oplus 0) \oplus 1$

$\Sigma = (1) \oplus 1$

$\Sigma = 0$

$Cout = AB + (A \oplus B)Cin$

$Cout = (1)(0) + (1 \oplus 0)1$

$Cout = 0 + (1)(1)$

$Cout = 1$

Q2:- What are the half-adder inputs that will produce the following output $\Sigma = 0$, $Cout = 0$.

Ans:-

$\Sigma = 0$, $Cout = 0$

$A = ?$ $B = ?$

for Σ and Cout both to be zero the A and B must be zero.

$A = 0$

$B = 0$

$\Sigma = A \oplus B$

$0 = 0 \oplus 0$

Ans.

$Cout = AB$

$Cout = 0.0$

Q3:- Determine the output of a full adder for the following inputs.

Ans:- $A = 1$, $B = 1$, $Cin = 1$

$\Sigma = (A \oplus B) \oplus Cin$

$\Sigma = (1 \oplus 1) \oplus 1$

$\Sigma = (1)$

Ans.

$Cout = AB(A \oplus B)Cin$

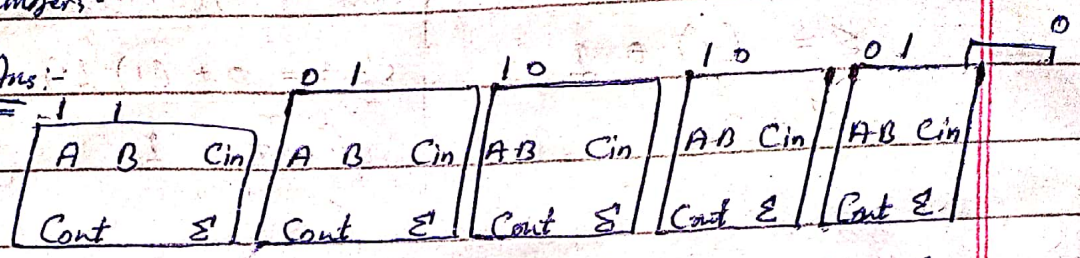
$Cout = 1.1 + (1 \oplus 1)1$

$Cout = 1 + (0)1$

$Cout = 1$

Q4:- For the parrell adder in figure 01 determine the complete sum by analysis of the logical operation of the circuit. verify your result by longhand addition of two input numbers.

Ans:-



A = 1 0 1 1 0

B = 1 1 0 0 1

10 1 1 1 1 Ans.

QUESTION-5

PART 'A':-

When the Add/sub is high the input bits of will be complemented and the resulting Σ will be the subtraction of the input bits.

PART 'B'

When the Add/sub is low the input bits of B will not be changed and the circuit will work as a parrellal adder for the input bits.

Q 6:- For the circuit in Figure 02, assume the input are $\overline{Add}/sub = 1$, A = 1010, and B = 1101, what is the output.

Ans:-

$\overline{Add}/sub = 1$, A = 1010, B = 1101

for Σ_0 & $A_0 = 0$, $B_0 = 1 \oplus 1$, $C_{in} = 1$

$\Sigma_0 = 0 + 0 + 1 = 1$, $C_{out} = 0$

for $\Sigma_1 = A_1 = 1$, $B_1 = 1 = 1 \oplus 0$, $C_{in} = 0$

$\Sigma_1 = 1 + 1 + 0 = 0$; $C_{out} = 1$

for $\Sigma_2 = A_2 = 0$, $B_2 = 1 \oplus 1$, $C_{in} = 1$

$\Sigma_2 = 0 + 0 + 1 = 1$, $C_{out} = 0$

for $\Sigma_3 = A_3 = 1$, $B_3 = 1 \oplus 1$, $C_{out} = 0$

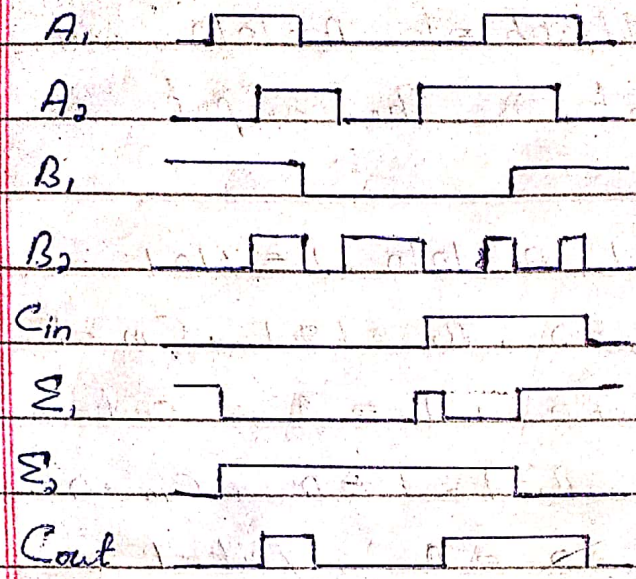
$\Sigma_3 = 1 + 0 + 0 = 1$, $C_{out} = 0$

$\Sigma = \Sigma_3 \Sigma_2 \Sigma_1 \Sigma_0 = 1101$, $C_{out} = 0$

Ans.

Q 7:- The input waveform in figure are applied to a 2-bit order Determine the waveforms for the sum and the output carry in relation to the inputs by constructing a timing diagram.

Ans:-



Q 8:-

$A_1 = 1010$, $A_2 = 1100$, $A_3 = 0101$

$A_4 = 1101$

$B_1 = 1001$, $B_2 = 1011$, $B_3 = 0000$, $B_4 = 0001$

Sol:-

A_4	A_3	A_2	A_1	+	B_4	B_3	B_2	B_1	=	Σ_5	Σ_4	Σ_3	Σ_2	Σ_1
1	0	1	1		0	0	1	1		0	1	1	1	0
1	1	1	0		0	0	0	0		0	1	1	1	0
0	0	0	1		0	0	1	0		0	0	1	1	1
1	1	0	0		1	0	1	1		1	0	1	1	1

$\Sigma_5 = 0\ 0\ 0\ 1$

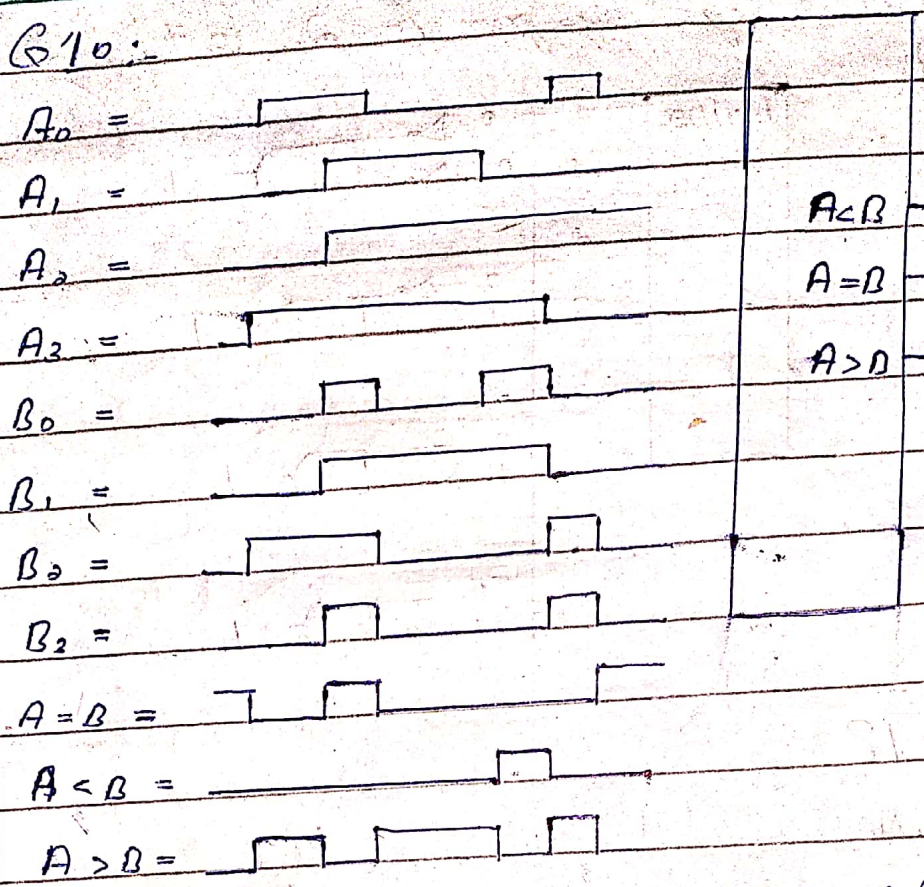
$\Sigma_4 = 1\ 1\ 0\ 0$

$\Sigma_3 = 1\ 1\ 0\ 1$

$\Sigma_2 = 1\ 1\ 1\ 1$

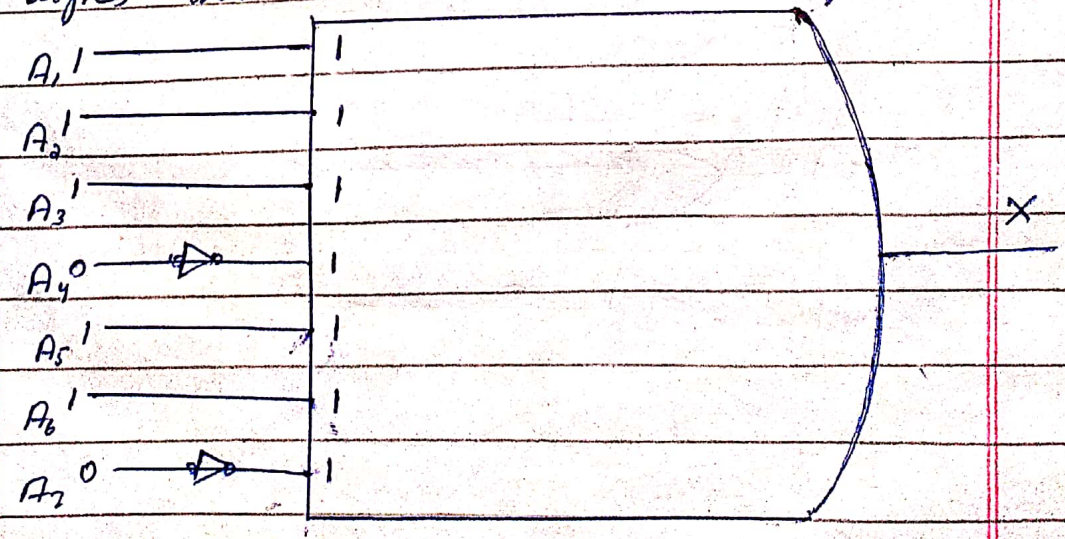
$\Sigma_1 = 0\ 1\ 1\ 1$

Q10:-



Q11:- Show the decoding logic for the following codes if an active-HIGH(1) output is required : 1110110

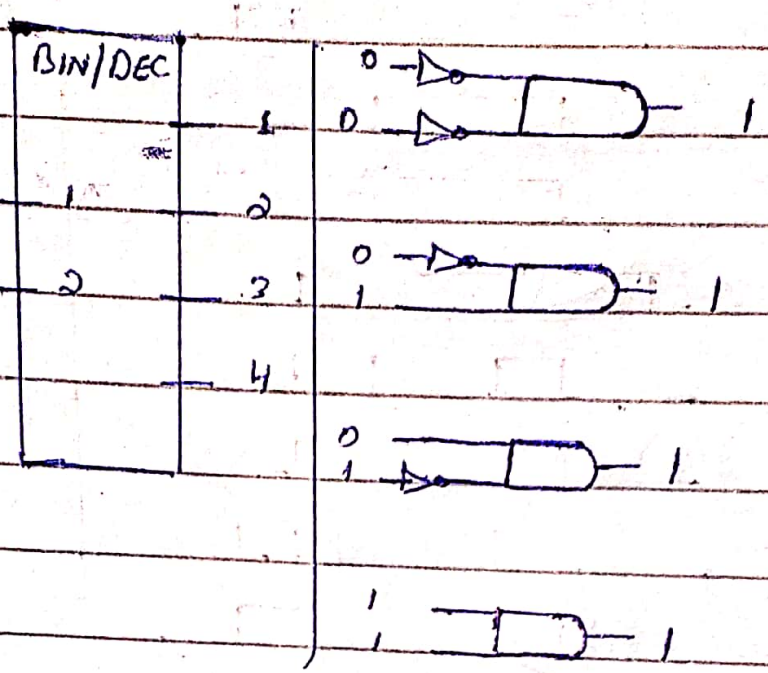
Ans:- For the output to be High for the given code 1110110 following is the decoding logics that can be used to decode the given code.



$X = \bar{A_7}\, A_6\, A_5\, \bar{A_4}\, A_3\, A_2\, A_1$ Ans.

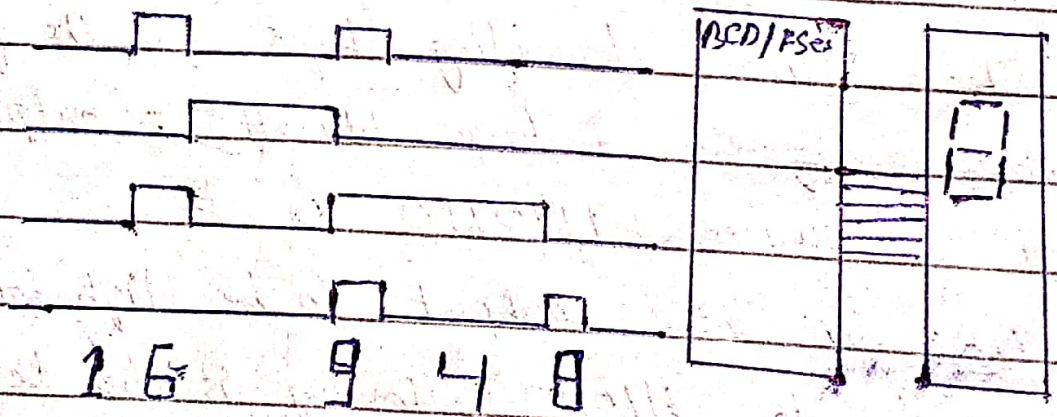
Q12:- Draw logic diagram for 2 to 4 line decode.

Ans:

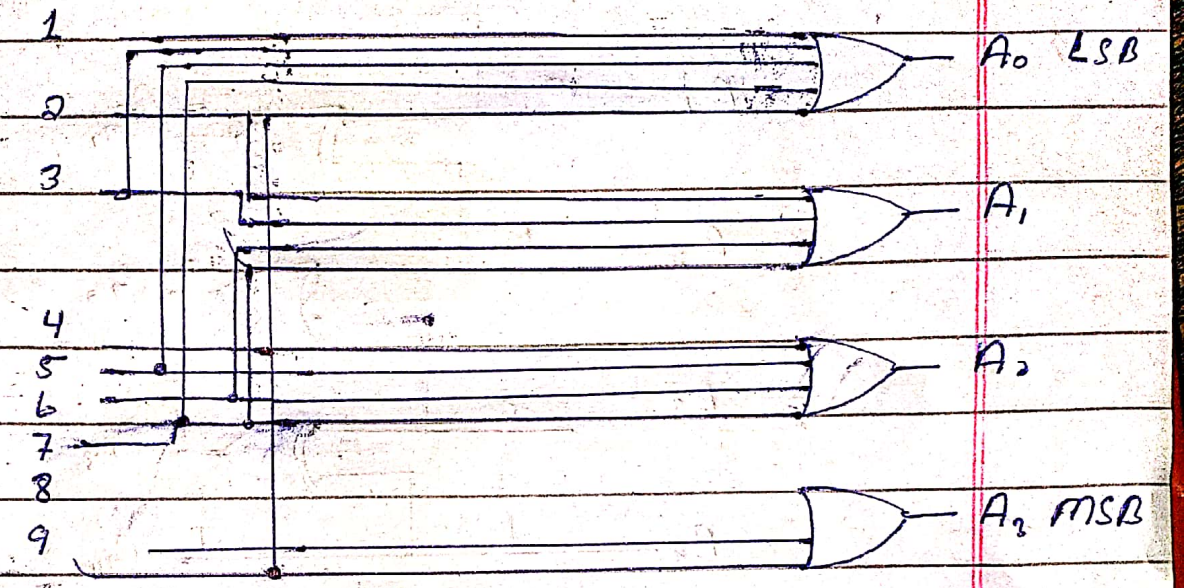


Q13:-

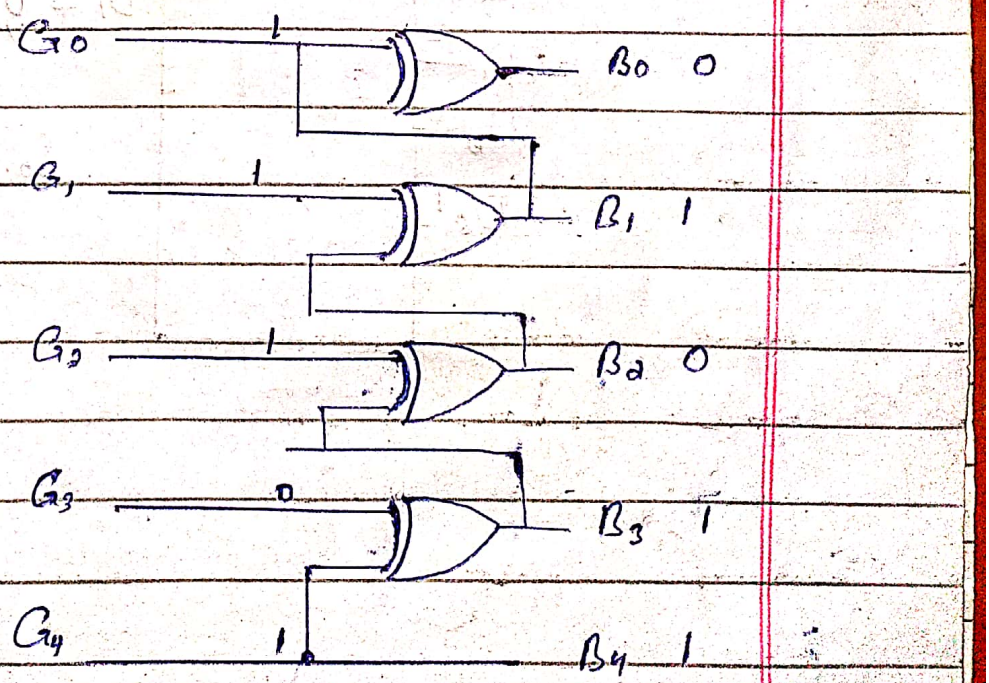
Ans:-



Q14:- Draw logic digram for decimal to BCD encode.



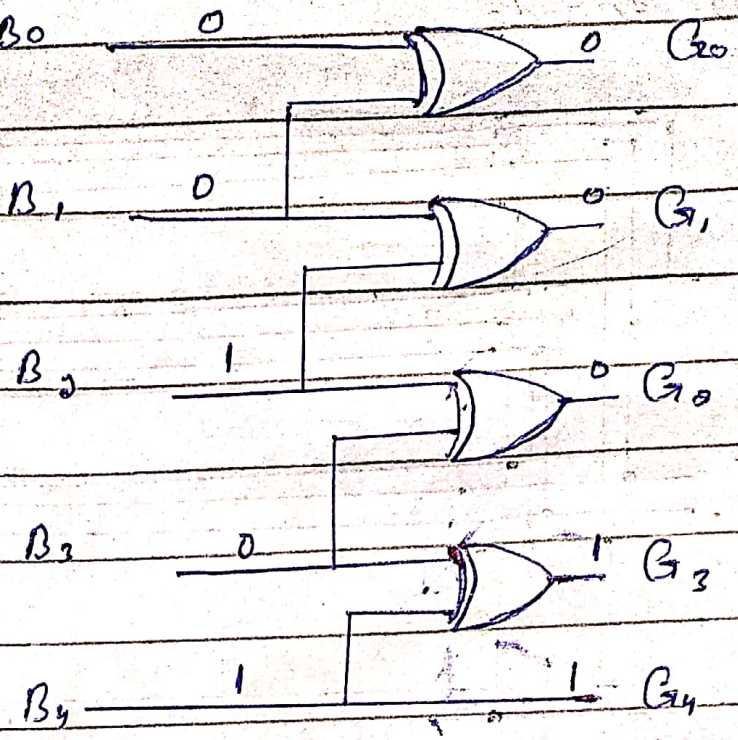
Q16:- Show the logic required to convert a 5-bit Gray code to binary and use that logic to convert the following Gray code words to binary 1011.



$1011_G = 1101_B$

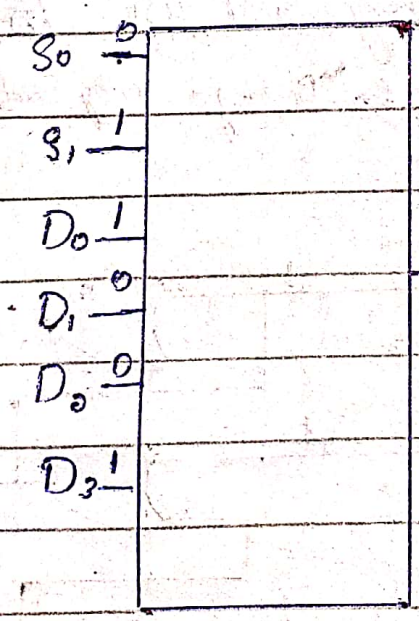
Q 15 :-

Ans :-



10100 = 1100

Q 17 :-

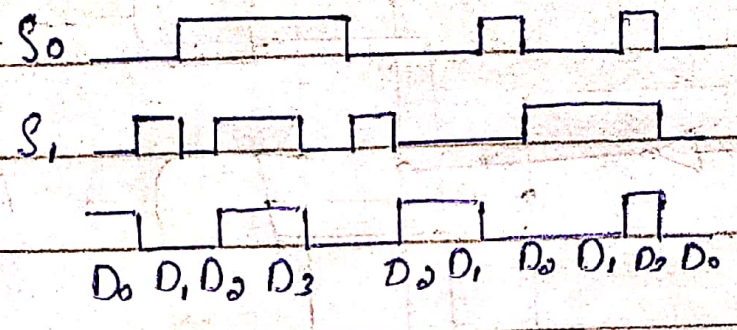


$D_1 = 0$

$S_0 . S_1 = 01 \Rightarrow 0$

Q18:-

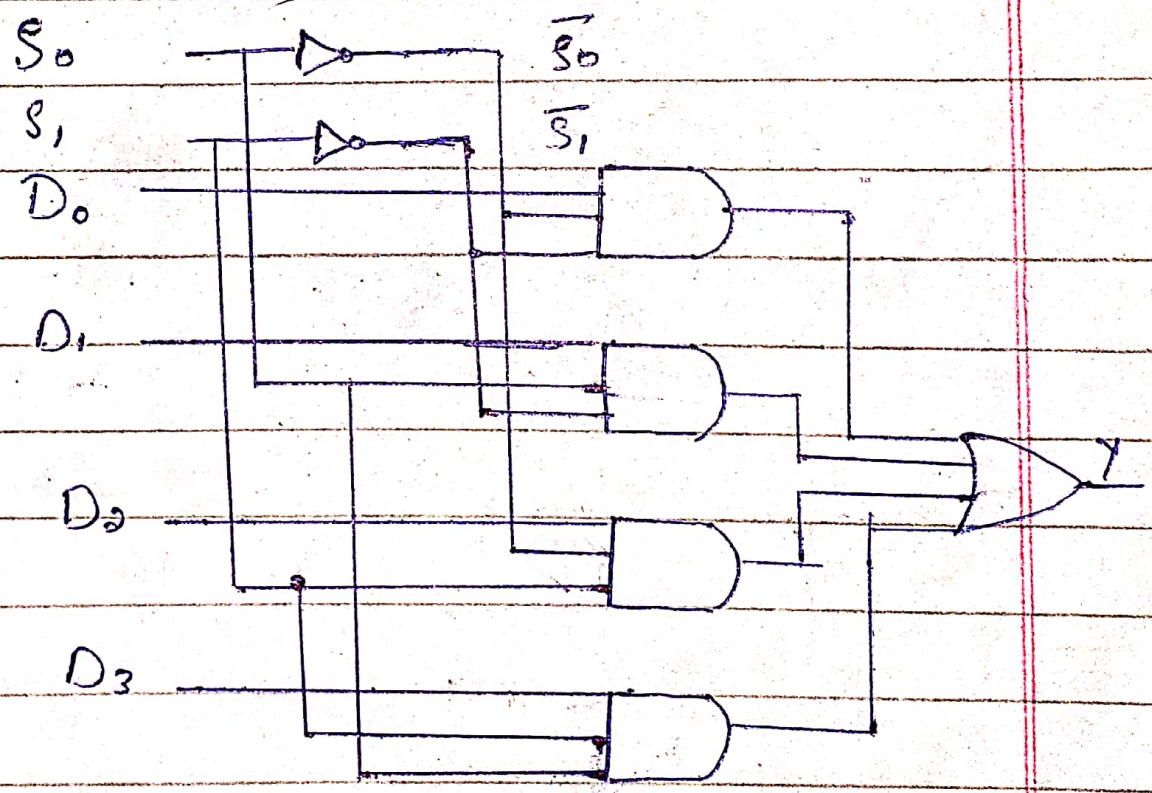
Ans:-



Q19:-

Draw logic diagram for 4 to 1 line multiplexer.

Ans:-



Q2o:

Ans:-