Department of Electrical Engineering
Assignment
Date: 20/04/2020

Course Details

Course Title: VLSI
Instructor: Sir Zulqarnain
Module:
Total Marks:

Student Details

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Part A (Objective Type)

1. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance??
   a. Static dissipation
   b. Dynamic dissipation ✔
   c. Both a and b
   d. None of the above.

2. Which type of MOSFETS Exhibits no current at zero gate voltage?
   a. Depletion MOSFET
   b. Enhancement MOSFET ✔
   c. Both a and b
   d. None of the above

3. CMOS circuits are constructed in such a way that all PMOS transistors must have either an input from the voltage source or from another
   a. PMOS transistor ✔
   b. NMOS transistor
   c. CMOS transistor
   d. BJT transistor

4. Delay which is equal to the time taken by a gate output transition to 0, from another value 1, x, or z is
   a. Rise delay
   b. Fall delay ✔
   c. Turn-off delay
   d. Turn-on delay

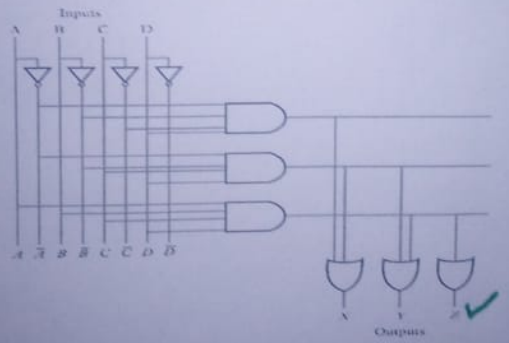
5. Which type of simulation model is used to check the timming performance of a design?
   a. Transistor level
   b. Gate level ✔
   c. Behavioral
   d. Switch level
   e. None of these

6. Which of the following statements is incorrect
   a. Some PLDs are programmed using electrically operated switches.
   ✔ b. Some PLDs are programmed using mechanical switches

Fill in the Blanks

Constant & Independent

7. In MOS devices, the current at any instant of time is _____of the voltage across their terminals.
8. For complex gate design in CMOS, OR function needs to be implemented by Parallel _____connections of MOS
9. In the following PLA, which output implements the logic function ABCD??



10. The term VLSI means a device containing between Mos and million transistors.

Part B (Subjective Type)

Q1.		In low power VLSI design clock gating technique will reduce power all time or it depends upon the input date? Is any chance, the computation power may increase?	(5)
Q2.	(a)	If we want to design an IC and I want that each and every transistor used in this IC should be optimized individually with less time. How it will be possible??	(5)
	(b)	While fabrication of NMOS or PMOS we usually use inorganic polymer. If we use organic polymer instead of inorganic polymer what will happen??	(5)
Q3.		Draw a stick diagram of a layout using that variable ordering F=	(5)

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Q(1) In Low VLSI design Clock gating Technique will reduce power all time or it depends upon the input gate? is any chance, the computation power may increase?

Ans=> Clock gating Technique is basically used for dynamic power reduction. After applying this Technique the main problem will be.

=> The number of Transistor count increase

=> Number of interconnect capacitance increase and hence delay may increase

=> static power may increase.

Q(2)
(A) If we want to design an Ic and I want that each and every Transistor used in this Ic should be optimized individually with less time. How it will be possible?

Ans=) It can be possible.

=> An Integrated circuit is a tiny silicon chip, less then centimeter in width. Among other things. The Ic contain arrays of Transistor that help process data. The more transistor there are in a ckt, the faster the data is processed. modern Technology has allowed data to be processed rapidly by increasing the number of Transistor and decreasing the size of the Ic.

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(B) While fabrication of Nmos & or Pmos we usually use inorganic polymer if we use organic Polymer instead of inorganic polymer what will happen?

Ans=> Typically we use inorganic Polymer for fabrication of Nmos or Pmos Because they contain with carbon-atom & back bone.

=> And they have high ~~quality~~ ability of noise and this make them better conductor

=> If we use organic polymer instead of inorganic polymer for febrication of Nmos & Pmos.

=> So they have become a poor conductor for electricity & heat.

CLO3) Draw a Stick diagram of Layout using that variable ordering

~~$F = ABC + ABD$~~

$F = ACD + ABD$

Ans=> Nmos: + -> Parallel
. -> series

Pmos: . -> Parallel
+ -> series

$F = ACD + ABD$

$= AD(C + B)$

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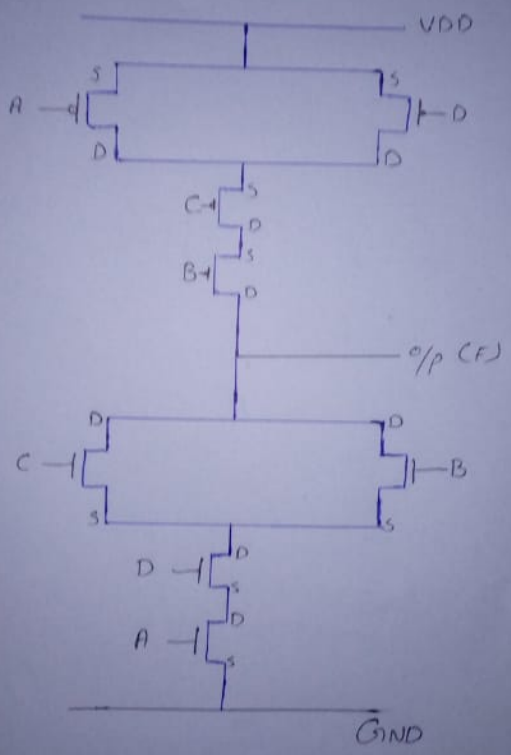

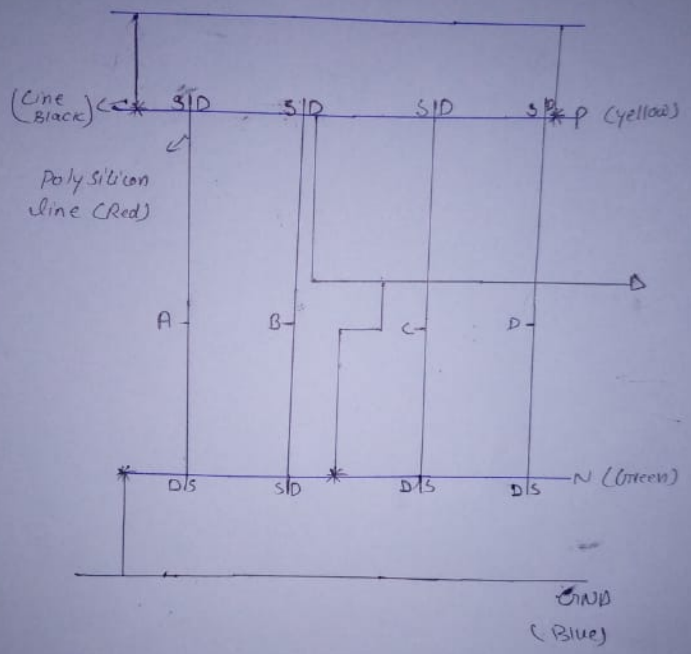
(Cine Black)
S/D
S/D
S/D
S/D
P (yellow)
Poly silicon line (Red)
A
B
C
D
D/S
S/D
D/S
D/S
N (Green)
GND
(Blue)