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Question # 1

Give answers to each of the following:

(a) Discuss the concept of word, addressable units, and unit of transfer for internal memories?

Ans) **WORD:** The "natural" unit of organization of memory. The size of the word is typically equal to the number of bits used to represent an integer and to the instruction length. Unfortunately there are many exceptions. For example, the CRAY C90 has a 64-bit word length but uses a 46-bit integer representation. The VAX has a stupendous variety of instruction lengths, expressed as multiples of bytes, and a word size of 32 bits.

ADDRESSIBLE UNITS: In some systems, the addressable unit is the word. However many systems allow addressing at the bytes level. In

any case, the relationship between the length in bits A of an address and the number N of addressable units is $2^A = N$.

UNIT OF TRANSFER:

For main memory, this is the number of bits read out of or written into memory at a time. The unit of transfer need not equal a word or an addressable unit. For external memory, data are often transferred in much larger units than a word, and these are ~~#eff~~ referred to as blocks.

(b) How least recently used (LRU) & least frequently used (LFU) replacement algorithms are implemented for a cache memory with two-way set associative mapping?

Ans) **LEAST-RECENTLY-USED (LRU):**

In this technique, the block in the set which has been in the cache longest with no reference to it, is selected for the replacement. Since we assume that more recently used memory locations are more likely

to be referenced again. This technique can be easily implemented in the two-way set associative cache organisation.

LEAST-FREQUENTLY-USED (LFU):

In this technique, the block in the set which has the fewest references is selected for the replacement.

(c) How read & write operations are performed in SRAM cell?

Ans) ## READ OPERATION:

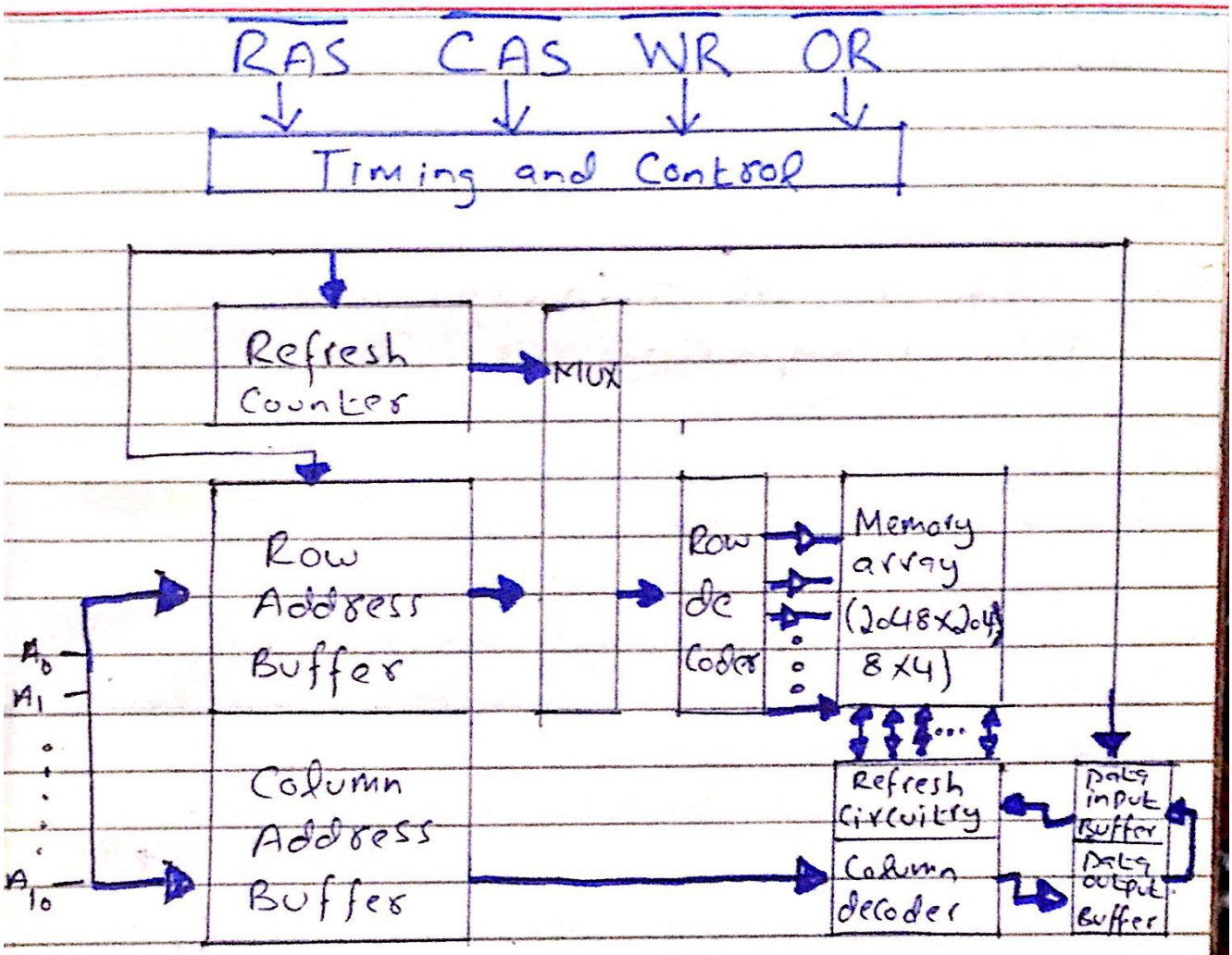
In SRAM, for any operation to be performed, the word line should be high. To perform read operation initially. A voltage signal is applied to the bit line high voltage 1, low voltage 0.

WRITE OPERATION:

Consider the memory bits consists of $Q=0$ and $Q'=1$.

Read and write operation is performed in SRAM cell by WL and BLs. SRAM cell operates in the active mode where cell performs read & write operation and Standby mode or idle mode where cell is not performing any activity. In Stand by mode WL = 0 and two bit-lines are pulled to ground. only minimum voltage is applied on the cell to hold the data. This mode is useful for saving power Consumption of the cell. ~~A~~ SRAM cell Consumes maximum power during write operation. where it is required full swing voltage on bit-lines.

(d) Discuss 16-Mbit DRAM (4M×4) organization in detail?



Typical 16-Mbit DRAM (4M x 4)

Because only 4 bits are read/written to this DRAM, there must be multiple DRAMs connected to the memory controller to read/write a word of data to the bus.

All the DRAMs require a refresh operation. A simple technique for refreshing is, in effect, to disable the DRAM chip, while all data ~~store~~ cells are ~~kept~~ refreshed. The refresh

Counter steps through all of the row values. This causes each cell is row to be refreshed.

(e) What are the reason for DVD's greater capacity over CD?

Ans) The DVD's greater capacity is due to three differences from CDs;

1) Bits are packed more closely on a DVD. The spacing between loops of a spiral on a CD is 1.6 μm and the minimum distance between pits along the spiral is 0.834 μm. The DVD uses a laser with shorter wavelength and achieves a loop spacing of 0.74 μm and a minimum distance between pits of 0.4 μm. The result of these two improvements is about a seven-fold increase in capacity, to about 4.7 GB.

2) The DVD employs a second layer of pits and lands on top of the first layer. A dual-layer DVD has a semi-reflective layer on top of the reflective layer, and by adjusting focus, the layers in DVD drives can reach each layer separately. This

technique almost doubles the capacity of the disk, to about 8.5 GB. The lower reflectivity of the second layer limits its storage capacity so that a full doubling is not achieved.

3) The DVD-ROM can be two sided, whereas data are recorded on only one side of a CD. This brings total capacity up to 17 GB.

Question # 2

Differentiate each of the following in detail:

(a) EEPROM and flash memory?

EEPROM:

- EEPROM devices can erase any byte of memory at any time.
- EEPROM uses Nor type memory.
- EEPROM is byte-wise erasable.

FLASH MEMORY:

- Flash memory can only erase an entire chunk, or "sector" of memory at a time.
- Flash memory uses NAND type memory.
- Flash is ~~byte~~ block-wise erasable.

(b) Hard failure and soft error in semiconductor memories?

Ans) **HARD FAILURE:**

A hard failure is a permanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically between 0 & 1. Hard errors can be caused by ~~hard~~ harsh environment abuses, ~~manufa~~ manufactoring defects and wear.

SOFT ERROR:

Soft error is a random, nondestructive even that alters the contents of one or more ~~mem~~ memory cells without damaging the memory. Soft errors can be caused by power supply problems or alpha particels. These particles result from radioactive decay & are distressingly common because radioactive nuclei are found in small quantities in nearly all materials.

Both hard and soft errors are clearly undesirable, & most modern main memory systems include logic for both detecting and correcting errors.

(c) Read and write Mechanisms for magnetic disk?

Ans) **READ &**

The traditional read mechanism exploits the fact that a magnetic field moving relative to a ~~coil~~ Coil produces an electrical current in the coil. When the surface of the disk passes under the head it generates a current of the same polarity as the one already recorded. The structure of the head for reading is in this case essentially the same as for writting. Such single heads are used in floppy disk systems and in older ~~rigit~~ rigid disk System Contemporary rigid disk System. Use a different read mechanism requiring a separate read head positioned for convenience close to the write head. The read

head consists of a partially shielded magnetoresitive (MR) ~~Sen~~sensor. The MR material has an electrical resistance that depends on the direction of the magnetization of the medium moving under it. By passing a current through the MR Sensor, resistance changes are detected as voltage signals. The MR design allows high frequency operation, which equates to greater storage densities and operating speeds.

WRITE:

The write mechanism exploits the fact that electricity flowing through a coil produces a magnetic field. Electric pulses are sent to the write ~~hold~~ head and the resulting magnetic patterns are ~~recording~~ recorded on the surface below, with different patterns for positive and negative currents. The write head ~~if~~ itself is made of easily magnetizable material and is in the shape of a rectangular doughnut with a

gap along one side and a few turns of conducting wire along the opposite side. An electric current in the wire induces a magnetic field across the gap, which in turn magnetize a small area of the recording medium, Reversing the direction of the current reverses the direction of the ~~magnetic~~ magnetization on the recording medium.

(d) Parallel access and independent access ~~KAD~~ RAID Schemes?

Ans) **PARALLER ACCESS :**

All member disks participate in the execution of every I/o request. Typically, the spindles of the individual drives are synchronized. So that each disk head is in the same position on each disk at any given time.

INDEPENDENT ACCESS :

Each member disk operates independently, so that separate I/o requests can be satisfied in parallel.

(e) HD DVD and Blue-ray DVD?

Ans) HD DVD players have been much cheaper than Blue-ray machines, but Blu-ray discs have more storage space and more advanced protections against piracy. Both versions deliver sharp resolution. Blu-Ray has 25 GB capacity (50GB for dual layer) & is more expensive. HD DVD has 15 GB (30 GB for dual layer) and is cheaper than Blu-Ray.

Question # 3

Write note on each of the following:

(a) Memory access methods?

Ans) These are 4 types of memory Access method.

1) **SEQUENTIAL ACCESS:**

In this method, the memory is accessed in a specific linear sequential manner, like accessing in a single linked List. The access time depends on the location of the data. Application

of this sequential memory access are magnetic tapes, magnetic disk and optical memories.

2) RANDOM ACESS:

In this method, any location of the memory can be accessed randomly like accessing in Array. Physical location are independent in the access method. Applications of this random memory access are RAM and ROM.

3) DIRECT ACCESS:

In this method, the particular location of the memory can be accessed directly like accessing in Array. This method is a ~~Combined~~ Combination of above two access methods. The access time depends on both the memory organization and characteristics of Storage technology. The access is semi-random or direct. Application of this direct memory access ~~is~~ is magnetic hard disk, read/write header.

4) Associate Access:

In this memory, a word is accessed rather than its address. This access method is a special type of random access method. Application of this direct memory access is cache memory.

(b) Princple of locality?

Ans) The principle of locality states that data in the vicinity of a referenced word are likely to be referenced in the near future.

OR

An implication of locality is that we can predict with reasonable accuracy what instructions and data a ~~prog~~ program will use in the near future based on its accesses in the recent past.

(c) Possible approaches to cache Coherency?

Ans) Possible approaches to cache coherency include the following;

- **Bus Watching with Wire through:**
Each cache controller monitors the ~~adde~~ address lines to detect write operations to memory by other bus masters. If another master writes to a location in shared memory that also resides in the cache memory, the cache controller invalidates that cache entry. This strategy depends on the use of a write-through policy by all cache controllers.

- **Hardware Transparency:**
Additional hardware is used to ensure that all updates to main memory via cache are reflected in all caches. Thus, if one processor modifies a word in its cache, this update is written to main memory. In addition any matching words in other caches are similarly updated.

- **Non-Cacheable Memory:**
Only a portion of main memory is shared by more than one processor, and this is ~~designed~~ designated as non-cacheable. In such a system all accesses to shared memory are

Cache misses, because the shared memory is never copied into the Cache. The non-cachable memory can be identified using chip-select logic or high-address bits.

(d) Practical Issues peculiar to SSDs?

Ans) There are two practical issues peculiar to SSDs that are not faced by HDDs:

- SDD performance has a tendency to slow down as the device is used
  - The entire block must be read from the flash memory and placed in a RAM buffer.
  - Before the block can be written back to flash memory, the entire block of flash memory must be erased.
  - The entire block from the buffer is now written back to the flash memory.
- Flash memory becomes unusable after a certain number of writes:
  - Techniques for Prolonging life:

- Front-ending the flash with a cache to delay and group write operations.
- Using wear-leveling algorithm that evenly distribute writes across block of cells.
- Bad-block managment techniques.
- Most flash devices estimate their own remaining lifetimes so system can anticipate failure and take preemptive action.

(e) CD read and write operation?

Ans) **READ:**

Information is retrieved from a CD or CD-ROM by a low-powered laser housed in an optical-disk player, or drive unit. The laser shines through the clear polycarbonate while a motor spins the disk past it. The intensity of the reflected light of the laser changes as it encounters a pit. Specifically if the laser ~~become~~ beam falls on a pit, which has a some what rough surface, the light scatters & a low intensity

is reflected back to the source. The areas between pits are called lands. A land is a smooth surface, which reflects back at higher intensity. The change between pits and lands is detected by a photo sensor & converted into a digital signal. The sensor tests the surface at regular intervals. The beginning or end of a pit represents a 1; when no change in elevation occurs between intervals as 0 is recorded.

WRITE :

Recall that on a magnetic disk, information is recorded in concentric tracks. With the simplest constant angular velocity (CAV) system, the number of bits per track is constant. An increase in density is achieved with multiple zoned recording in which the surface is divided into a number of zones, with zones farther from the center. Although this technique increases capacity, it is still

not optimal.

Question # 4

Part (a)

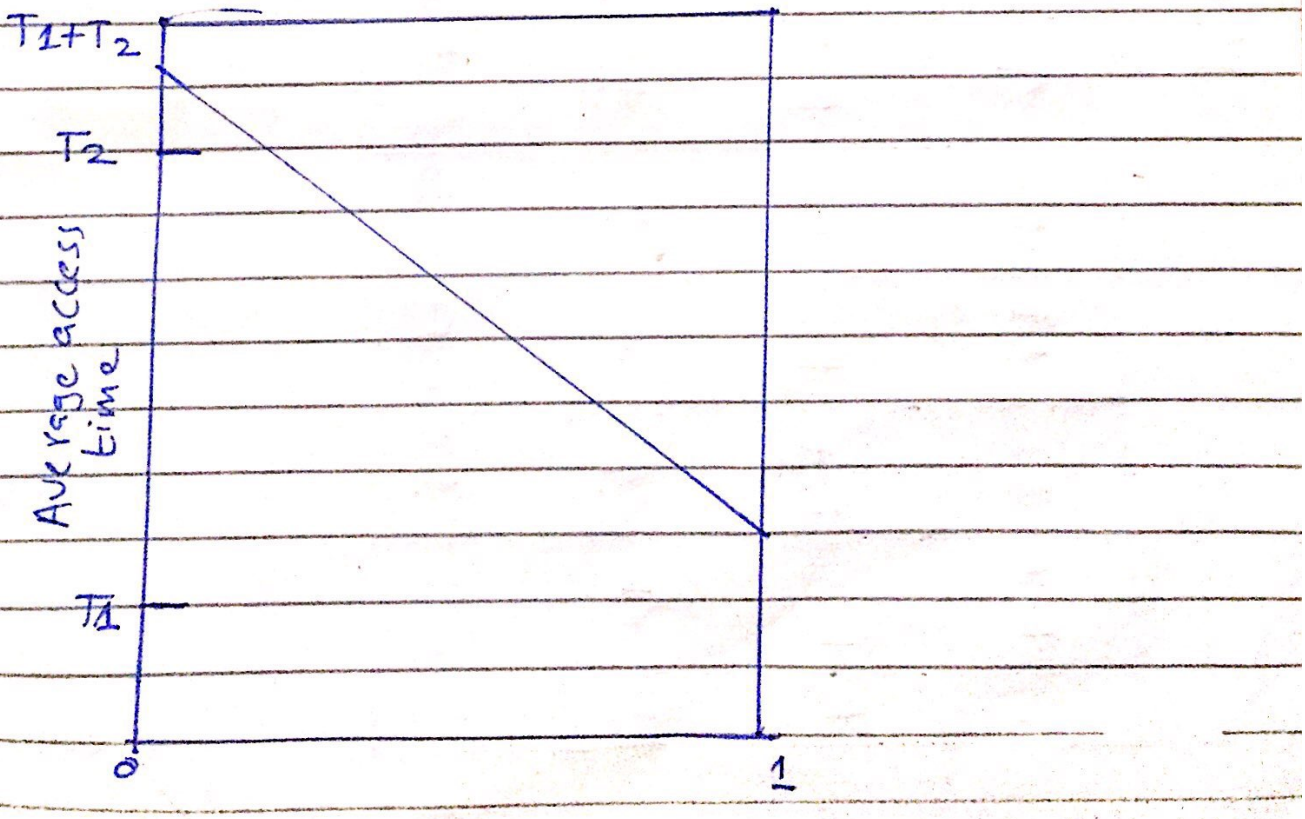
Solution :

In our example, suppose 95% of the memory access are found in level 1. Then the average time to access a word can be expressed as

$(0.95)(0.01\ \mu s) + (0.05)(0.01\ \mu s + 0.1\ \mu s)$

$= 0.0095 + 0.0055 = 0.015\ \mu s$

The average access time is much closer to $0.01\ \mu s$ than to $0.1\ \mu s$, as desired.



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Part (b)

Total block in the cache =
8K bytes = $2^3 \times 2^{10} / 2^4 = 2^9 = 512$

Number of set = number of block in cache / 2

Number of set = 512 / 2

Number of set in cache = 256

Number of set in cache = 2^8

Number of set = 8

Size block = 16 = 2^4

Size of memory = $2^6 \times 2^{10} = 2^{16}$

Tag = Size of memory − set size of block

Tag = 26 − 8 − 4

Tag = 14

tag	set	Size of block
14	8	4

~~Tag / set~~ word(2)
~~9 / 13~~

177H/0EEH

Tag / set / word(2) 177H/0EEH/3H
9 / 13 /

Part (C) 21

Position	12	11	10	9	8	7	6	5	4	3	2	1
Bits	D8	D7	P6	D5	C8	D4	D3	D2	C4	D1	C2	C1
Block	1	0	1	0	—	1	0	1	—	0	—	—
Codes	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001

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The Check bit one in bit numbers 8, 4, 2 and 1 Check bit 8 Calculated by values in bit numbers 12, 11, 10 and 9 = 0
Check bit 4 Calculated by values in bit 12, 7, 6, & 5 = 1
Check bit 2 Calculated by values in 11, 10, 7, 6 & 3 = 0
Check bit 1 Calculated by values in 11, 10, 9, 7, 5 & 3 = 0
Thus the check bit are = 0010