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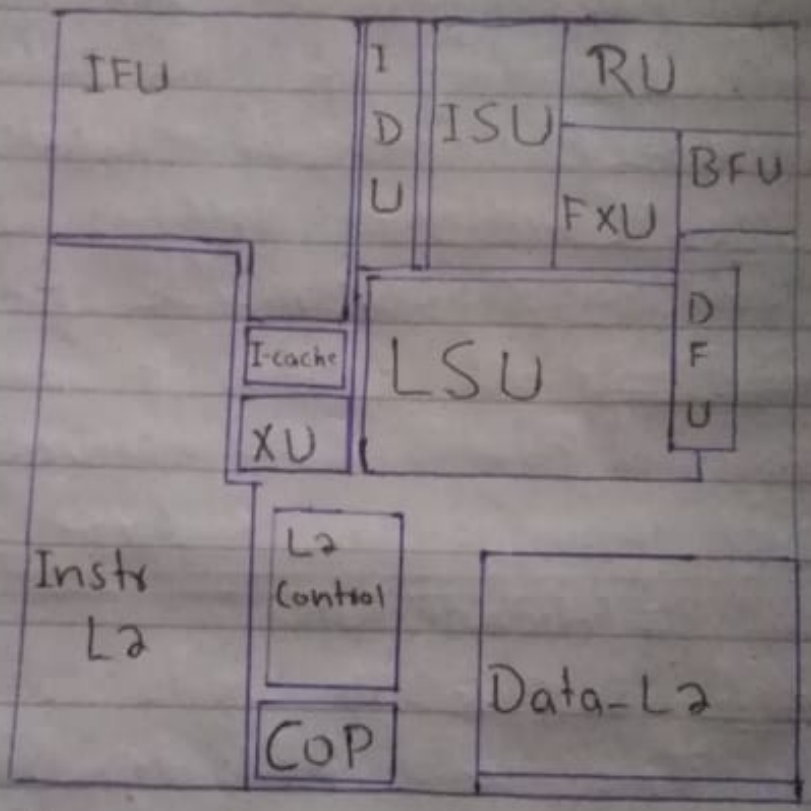
Computer Architecture



Function of each Subarea:-

- ISU: (instruction sequence unit)
  Determine the sequence in which instruction are executed in what is referred to as a superscalar architecture.
- IFU :- (instruction fetch unit)
  Logic for fetching instruction

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- **IDU:-** (instruction decode unit)
  The IDU is feed from the IFU buffers, and is responsible for the parsing and decoding of all z/Architecture operation codes.
- **LSU:-** (Load-store unit)
  It is responsible for handling all types of operand accessies of all lengths, modes, and formats as defined in the z/Architecture.
- **XU:-** (translation unit)
  This unit translates logical addresses from instruction into physical addresses in main memory.
- **FXU:-** (Fixed-point unit)
  The FXU executes fixed-point arithmetic operation.
- **BFU:-** (binary floating-point unit)
  The BFU handles all binary and hexadecimal floating-point

operations, as well as fixed-point multiplication operations.

- DFU :- (decimal floating-point unit)
  The DFU handles both fixed-point and floating-point operations on number that are stored as decimal digits.
- RU :- (recovery unit)
  The RU keeps a copy of the complete state of the system that includes all registers, collects hardware fault signals etc.
- COP :- (dedicated co-processor)
  The COP is responsible for the data compression and encryption function for each core.
- I-Cache :-
  This is a 64-KB L1 instruction cache allowing IFU to prefetch instructions before they are needed

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- **L2 Controls:-**
  This is a control Logic that manages the traffic through the two L2 caches.
- **Data L2:-**
  A 1-mB L2 data cache for all memory traffic otherss than instructions.
- **Instr-L2:-**
  A 1mB L2 instruction cache.

Ans(B) **IAS Operation:-**

The IAS operates by sepetitively performing an instruction cycle. Each instruction cycle consists of two subcycles.

1. Fetch cycle:-

During fetch cycle the opcode of the next instruction is Loaded into the IR and the address portion is Loaded

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into the MAR. This instruction may be taken from the IBR or it can be obtained from memory by loading a word into the MBR and then down to IBR, IR and MAR.

2. Execute cycle:-

Control circuitry interpret the opcode and executes the instruction by sending out the appropriate control signals to cause data to be moved or an operation to be performed by the ALU

Ans(c) Embedded System:-

The term embedded system refers to the use of electronics and software within a product, as opposed to a general purpose computer, such as a Laptop or desktop system. Today many devices that

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use electric power have an embedded computing system.

Different embedded systems used in every day life are:
Cell phones, digital cameras, video cameras, calculators microwave ovens, home security systems, washing machines lighting systems printers etc.

Ans(D) Different desktop applications that require the great power of contemporary microprocessor based system are:

- Image processing
- Three dimensional rendering
- speech recognition
- video conferencing
- multimedics authoring
- voice and video annotation of files
- Simulation modeling

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Ans(a) The techniques used in contemporary processors to increase speed are following

(*) Pipelining :-

Pipelining enables a processor to work simultaneously on multiple instructions by performing a different phase of each of the multiple instructions at the same time.

(*) Branch predication :-

Branch predication potentially increase the amount of work available for the processor to execute.

(*) Superscalar Execution :-

This is the ability to issue more than one instruction in every processor clock cycles. In effect multiple parallel pipelines are used.

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(*) Data flow analysis:-

The processor analyzes which instructions are dependent on each others result, or data, to create an optimized schedule of instructions.

(*) Speculative execution:-

This enables the processor to keep its execution engines as busy as possible by executing instruction that that are likely to be needed.

Ans(F) The problems created due to increase in clock speed and Logic density of processor are:

•Power:-

As the density of Logic and clock speed on a chip increase so does the power density The difficulty of dissipating the heat generated on high-density high speed chips is becoming a

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Serious design issue.

- Rc delay:-

The speed at which electrons can flow on a chip between transistors is limited by the resistance and capacitance of the metal wires connecting them specifically, delay increases as the Rc product increases.

- Memory latency and throughput:-

Memory access speed (latency) and transfer speed (throughput) lag processor speeds.

Ans(6) Consider a program running on a single processor such that a fraction (1-f) of the execution time involves code that is inherently sequential and a fraction f that involves code that is infinitely parallelizable with no

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Scheduling overhead. Let T be the total execution time of the program using a single processor. Then the speed up using a parallel processor with N processor that fully exploits the parallel portion of the program is a follows;

$$\text{Speed up} = \frac{\text{Time to execute program on a single processor}}{\text{Time to execute program on N parallel processor}}$$

$$\text{Speed up} = \frac{T(1-f)+Tf}{T(1-f)+\frac{Tf}{N}} = \frac{1}{(1-f)+\frac{f}{N}}$$

Ans(#) Multicore :-

- The use multiple processors on the same chip, also referred to as multiple cores or multicore, provides the potential to increase performance without increasing the clock rate.
- If the software can support the effective use of multiple processors,

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Than doubling the number of processor almost double performance.
• Two core chips were quickly followed by four-core chips, then 8, then 16, and so on.

MIC :-

• The Leap in performance as well as the challenges in developing software to exploit such a large number of cores has led to the introduction of term called " many integreded core (MIC)"
• The multicore and MIC strategy involves a homogenous collection of general purpose processor on a single chips.

GPUs :- (GPGPU)

• A GPU is a core designed to perform parallel operations on graphics data it is found on a plug-in graphics card.

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- It is used to encode and render 2D and 3D graphics as well as process video.
- GPUs perform parallel operations on multiple sets of data, they are increasingly being used as vector processors for a variety of applications that require repetitive computations.

Ans(1) Quick Path Interconnect (QPI) protocol Layer

(*) In this layer, the packet is defined as the unit of transfer.
(*) The packet contents definition is standardized with some flexibility allowed to meet differing market segment requirements.
(*) One key function performed at this Layer is a cache coherency protocol, which deals with making sure that main memory values held in multiple caches are consistent.

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Ans[1] Physical and Logical Architecture of PCIe :-

→ Root Complex

- It is also called "chipset" or a "host bridge" which connects the processor and memory subsystem to the PCI Express switch fabric comprising one or more PCIe and PCIe switch devices.
- The root complex acts as a buffering device, to deal with difference in data rates between I/O controllers and memory and processor components.

PCIe links from the chipset may attach to the following kinds of devices that implements PCIe:

→ Switch:-

The switch manages multiple PCIe streams.

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→ PCIe endpoint

An I/O device or controller that implements PCIe, such as a Gigabit ethernet switch, a graphics, disk interface etc.

→ Legacy endpoint:-

Legacy endpoint category is intended for existing designs that have been migrated to PCI Express, and it allows legacy behaviors such as use of I/O space and locked transactions.

→ PCIe/PCI bridge:-

Allows older PCI device to be connected to the PCIe-based system.

Q No 2

Ans(A) Structural components of Computer:-

There are four main structural components of computer.

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1. central processing unit (CPU)

It controls the operation of the computer and performs its data processing functions: often simply referred to as "processor".

2. Main memory :-

It stores data.

3. I/O :-

It moves data between the computer and its external environment.

4. System Interconnection :-

Some mechanism that provides for communication among CPU, main memory, and I/O. A common example of system interconnection is by means of a "system bus".

Ans(B) The characteristics of computer family are as follows:

• similar or idential instruction sets:-

In some cases, the Lowers end of the ~~following~~ family has an

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instruction sets that is a subset of that of the top end of the family. This means that programs can move up but not down.

- **Similar or Identical operating system:-**

The same basic operating system is available for all family. ~~(This means that programs can move up but not down.~~ members.

- **Increasing Speed:-**

The rate of instruction execution increases in going from Lower to higher family members.

- **Increasing number of I/O Ports:-**

The number of I/O ports increases in going from Lower to higher family members.

- **Increasing memory size:-**

The size of main memory increases in going from Lower to higher family members.

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• Increasing cost:-

At a given point in time, the cost of a system increases in going from lower to higher family members.

Ans(c) • Stored program Computer:-

A fundamental design approach first implemented in the IAS Computer is known as the "stored-program concept". This idea is usually attributed to the mathematician John von Neumann.

The first publication of the idea was in a 1945 proposal by von Neumann for a new computer, the EDVAC (Electronic Discreate variable Computer).

In 1946, von Neumann and his colleagues began the design of a new stored-program computer, referred to as the "IAS" computer of the Princeton Institute for advanced studies. It consists of:

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→ A main memory, which stores both data and instructions.

→ An arithmetic and Logic unit (ALU) capables of operating on binary data.

Ans(D) Moores Law:-

- The famous Moore's Law which was proposed by Gordon Moore, observed that the number co-founder of intel, in 1965.
- Moore observed that the number of transistors that could be put on a single chip was doubling every year, and correctly predicted that this pace would continue into the near future.
- The consequences of moors Law are,

1. The cost of computer Logic and memory ciricutry has fallen at a dramatic rate.
2. The computer becomes smaller, making it more convenient to place in a variety of environments.

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3. There is a reduction in power requirements.

4. The interconnections on the integrated than circuit are much more reliable than solded connections

Ans(E) **Instruction Cycle State Diagram.**

The states in instruction cycle state diagram are follows,

- **Instruction address calculation (Iac):-**

Determine the address of the next instruction to be executed. Usually, this involves adding a fixed number to the address of the previous intruction.

- **Instruction fetch (If):-**

Read instruction from its memory Location into the processor.

- **Instruction operating decoding (iod):-**

Analyze instruction to determine type of operating to be performed and operand(s) to be used.

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- Operand address calculation (OAC):-

If the operation involves reference to an operand in memory or available via I/O, then determine the address of the operand.

- Operand fetch (OF):-

Fetch the operand from memory or read it in from I/O.

- Data operand:-

Perform the operation indicated in the instruction.

- Operand store:-(OS)

Write the result into memory or out to I/O.

Ans (F) Classes of interrupts:

(*) Program :-

It is generated by some condition that occurs as a result of an instruction execution, such as arithmatic overflow, division by zero attempt to execute an

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illegal machine instruction, or reference outside a user's allowed memory space.

(*) Timer:-

It is generated by a timer within the processor. This allows the operating system to perform certain function on a regular basis.

(*) I/O:-

It is generated by an I/O controller, to a single normal completion of an operation, request service from the processor, or to signal a variety of error conditions

(*) Hardware failure:-

it is generated by a failure such as power failure or memory parity error.

Ans(6) Bus Interconnection Schemes:-

The most common computer interconnection structures are based on the use of one or more

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System buses

A system bus consists typically of about fifty to hundreds of seperate lines. The line can be classified into three functional groups data, address, and control lines

→ Address Lines

The address lines are used to designate the source or destination of the data on the data bus. The width of the address bus determines the maximum possible memory capacity of the system

→ Data Lines

The data lines provide a path for moving data among system modules. These lines collectively are called the "data bus".

The data bus may consist of 32, 64, 128, or even more seperate lines the number of lines being referred to as "width of data bus"

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→ Control Lines:-

The control Lines are used to control the access to and the use of the data and address Lines. Because the data and address Lines are shared by all components there must be a means of controlling their use. Typical control lines include memory write, memory read, I/O write I/O reade, reset etc.

(Q#3)

Ans(A) Computer Architecture:-

Computer Architecture refers to those attributes of a system visible to a programmer or, put another way, those attributes that have a direct impact on the logical execution of a program. A term that is often used interchangeably with computer architecture is instruction set arcitecture (ISA)

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Computer Organization:-

Computer organization refers to the operational units and their interconnections that relize the architectural specifications.

Examples of architectural attributes include the instruction set, the number of bits used to represent various data types (e.g numbers, characters). I/O mechanisms and techniques for addressing memory.

Ans(B) **CISC:-**

The current x86 offering represents the result of decades of design effort on "complex instruction set Computers (CISCs)"

The x86 incorporectes the sophisticated design principles once found only on mainframes and sg super computers and sorves as an excellent example of CISc design.

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RISC:-

An alternative approach to processor design is the "reduced instruction set computer (RISC)

The ARM architecture is used in wide variety of embedded systems and is one of the most powerful and best-designed RISC-based systems on the market. In this section and the next, we provide a brief overview of these two systems.

Ans(c) Microprocessor:-

A microprocessor chips included registers, an ALU, and some sort of control unit or instruction processing logic. As transistor density increased, it become possible to increase the complexity of the instruction set architecture and ultimately to add memory and more than one processor. micro-processor chips, include multiple cores and substantial amount of cache memory.

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Microcontroller:-

A microcontroller is a single chip that contains the processor non-volatile memory for input and output (RAM), a clock, and an I/o control unit. The processor portion of the microcontroller has a much a lower silicon area than other microprocessors and much higher energy efficiency.

Ans(1) Cortex-A:-

The cortex-A and cortex -A50 are application processors, intended for mobile devices such as smart_phones and eBook readers, as well as consumer devices such as digital TV and home gateways (e.g DSL and cable Internet modems) These processors ran at higher clock frequency and support a memory management unit (mmu).

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Cortex-R :-

The cortex-R is designed to support real-time applications, in which the timing of events needs to be controlled with rapid response to events. They can run at a fairly high clock frequency and have very low response Latency.

Cortex-M :-

Cortex-M Series processors have been developed primarily for the microcontrolled domain where the need for fast, highly deterministic interrupt managements is coupled with the desire for extremely low gate count and lowest possible Power Consumption

Ans(F) Disabled Interrupt :-

A disabled interrupt simply means that the processor can and will ignore that interrupt

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request signal. If an interrupt During this time, it generally remain pending and will be checked by the processor after the processor has enabled interrupts. When a user program is executing and an interrupt occurs, interrupts are disabled immediately.

Nested Interrupts:-

Nested Interrupts is to allows interrupted of higher priority to cause a lower-priority interrupts handler to be itself interrupted. A user program begains at t=0. At t=10, a printer interrupt occours user information is placed on the system stack and execution continues at the printer "interrupt Service routine (ISR). While routines is still executing at t=15, a communication interrupt occours.

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Ans(a) Programming in Hardware:-

The "program" is the form of hardware and is termed as "hardwared program".

Suppose we construct a general purpose configuration of arithmetic and logic function. This set of hardware will perform various functions on data depending on control signal applied to the hardware. In the original case of customized hardware, the system accepts data and produces results.

Programming in Software:-

The new method of programming which is a sequence of codes or instructions is called software programming.

In this method programming is much easier. Instead of rewiring the hardware for each new program all we need to do is provide a new sequence of codes Each code

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is, in effect, an instruction, and part of the hardware interprets each instruction and generates control signals.

Q.4

Ans(A) 1: Here is a simple way to understand this problem.

Contents are divided up into two 5 bits instructions, LH and RH.

LH instruction = 010FA

opcode = 01

address = 0FA

RH instruction = 210FB

opcode = 21

address = 0FB

Since this in hexadecimal form, you have to convert this numbers to binary form.

LH instruction:-

01 = 0000001 = LOAD M(x)

M(x) refers to the memory address location 0FA.

The first 5 bits of 0BA should read LOAD M(0FA)

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RH instruction:-

21 = 00100001 - STOR M(x)

M(x) refers to the memory address Location 0FB.

The second 5 bits of 08A should read. STOR M(0FB)

Finally the assembly language code for 08A 01 0FA 21 0FB is

LOAD M(0FA)
STOR M(0FB)

1. In 08A address the M(0FA) transfer to the accumulator and transfer Contants of accumulator to memory Location 0FB.

2. In 08B address, the M(0FA) transfer to the accumulator and take next instruction from left half of M(08D).

3. In 08C address, the M(0FA) transfer to the accumulator and transfer Contants of accumulatoss to memory Location 0FB.

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Ans(c) Effective CPI:-

$CPI = (1 \times 46000) + (3 \times 33000) + (2 \times 16000) + (2 \times 9000)/100$

$CPI = 162000/100$

$\boxed{CPI = 1620}$

MIPS Rate:-

MIPS rate $= 60\,MHz/1620 \times 10^6$

MIPS rate $= 60 \times 10^6\,Hz/1620 \times 10^6$

MIPS rate $= 60\,Hz/1620$

$\boxed{MIPS\ rate = 0.037}$

Execution Time:-

$T = Ic/(MIPS \times 10^6)$

$T = 104000/(0.037 \times 10^6)$

$T = 104000/37 \times 10^3$

$T = 2811 \times 10^{-3}$

$\boxed{T = 2.811\,Sec}$

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Ans(D) (a) Since we have the same instruction mix, that mean the additional instructions for each task could be allocated appropriately between the instruction types. There fore, the following table be gotten

Instruction Type	CPI	Instruction Mix
Arithmetic and Logic	1	60%
Load store with cache hit	2	18%
Branch	4	12%
memory refrence with cache miss	12	10%

The average CPI = (1x0.6) + (2x0.18) + (4x0.12) + (12x0.1)

[CPI = 2.64]

There for, the CPI has been increased since the time for memory access

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is also increased.

b. MIPS = 400/2.64 = 152

There is a corresponding drop in the MIPS rate.

C. The speed up factor equals to the ratio of the execution times. Parallelizable is f=1, then Amdahl's Law decreases to speed up N=3. Therefore, the actual speedup is only about 75% of the theoritical speedup.

Ans(E) Six steps:-

(1) (a) The PC contains 300, the address of the first instruction. This value is loaded into the MAR.

(b) The value in location 300 (which is the instruction with the value 1940 in hexadecimal) is loaded into the MBR, and the PC is incremented. These two steps can be done in parallel.

(c) The value in the MBR is loaded into the IR.

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(2) (a) The address portion of the IR (940) is Loaded into the MAR

(b) The value in location 940 is Loaded into the MBR is Loaded into the Ac.

(3) (a) The value in the PC (301) is Loaded into the MAR.

(b) The value in location 301 (which is the instruction with the value 5941) is Loaded into the MBR and the PC is incrementeal.

(c) The value inthe MBR is Loaded into the IR.

(4) (a) The address portion of the IR (941) is loaded into the MAR.

(b) The value in location 941 is Loaded into the MBR.

(c) The old value of the Ac and the value of location, MBR are added and the result is stored in the Ac

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(5) (a) The value in the PC(300) is Loaded into the MAR

(b) The value in location 300 (which is the instruction with the value 2941) is Loaded into the MBR, and the PC is incremental

(c) The value in the MBR is Loaded into the IR

(6) (a) The address portion of the IR(941) is loaded into the MAR.

(b) The value in the Ac is Loaded into the MBR

(c) The value in the MBR is stored in location 941.

Ans(F) (a) 2^{24} = 16MBytes

(b)(1) If the local address bus is 32 bits, the whole address can be transferred at once and decoded in memory. However, Because the data bus is only 16bits, it will require 2 cycles to fetch a 32 bit instruction or operand