Suzyan Ahmad ID: 13062

Name : Suzyan Ahmad

ID : 13062

Program : BS. SE

Examination : Final Term

Instructor : Muhammad Amin

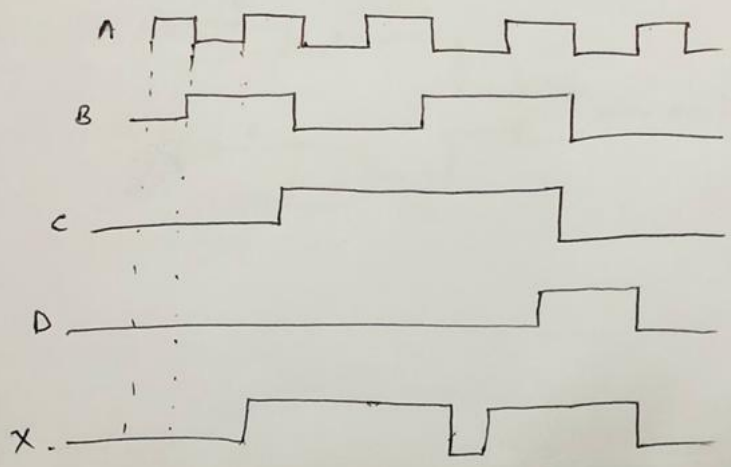
Semster : Summer 2020

Data : Sep. 26, 2020

Paper : Digital logico and Design

Q No: 01

Draw the logic circuit using the input (A, B, C, D) and output (x) wave forms in ~~Figer~~. Figure 01



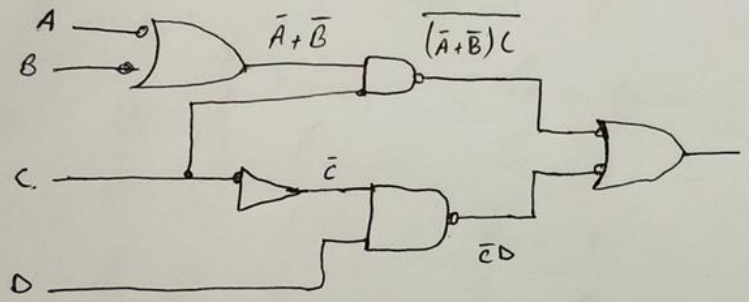
Sol:

The output expression for the circuit is developed in.

The SOP form indicates that the output

~~is low and~~ C

is High when A is Low and C is High or when B is Low and C is High or when C is Low and D is High.



$X = \overline{(\bar{A}+\bar{B})C} + \bar{C}D$

$= (\bar{A}+\bar{B})C + \bar{C}D$

$= \bar{A}C + \bar{B}C + \bar{C}D$

Q No 02

For the 4-input multiplexer data inputs are given as:

$D_0 = 0, \quad D_1 = 1, \quad D_2 = 0, \quad D_3 = 1$

Find the output Y if

(a) $S_0 = 1$ $S_1 = 0$

(b) $S_0 = 0$ $S_1 = 1$

(c) $S_0 = 1$ $S_1 = 1$

(d) $S_0 = 0$ $S_1 = 0$

Sol:- A 4×1 Mux has 4 input lines (D_0, D_1, D_2, D_3) two select input (S_0 and S_1) and one output line Y.

if $S_1 S_0 = 00$ then $Y = D_0$

$S_1 S_0 = 01$ then $Y = D_1$

$S_1 S_0 = 10$ then $Y = D_2$

$S_1 S_0 = 11$ then $Y = D_3$

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Data input		output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

When these terms are ORed. the total expression for the data output is

$$Y = D_0 \bar{S}_1 \bar{S}_0 + D_1 \bar{S}_1 S_0 + D_2 S_1 \bar{S}_0 + D_3 S_1 S_0$$

Q no : 03

For the circuit in figure 02, assume the input one $\overline{Add}/Subt = 1$ A = 1010 and B = 1101 what is the output.

Ans:- A ripper carry adder is one in which the carry output of each full-adder is connected to the carry input of the next higher-order stage. The sum and the output carry of any stage cannot be produced until the input carry occurs. This causes a time delay in the addition process as illustrated in figure The carry propagation delay for each

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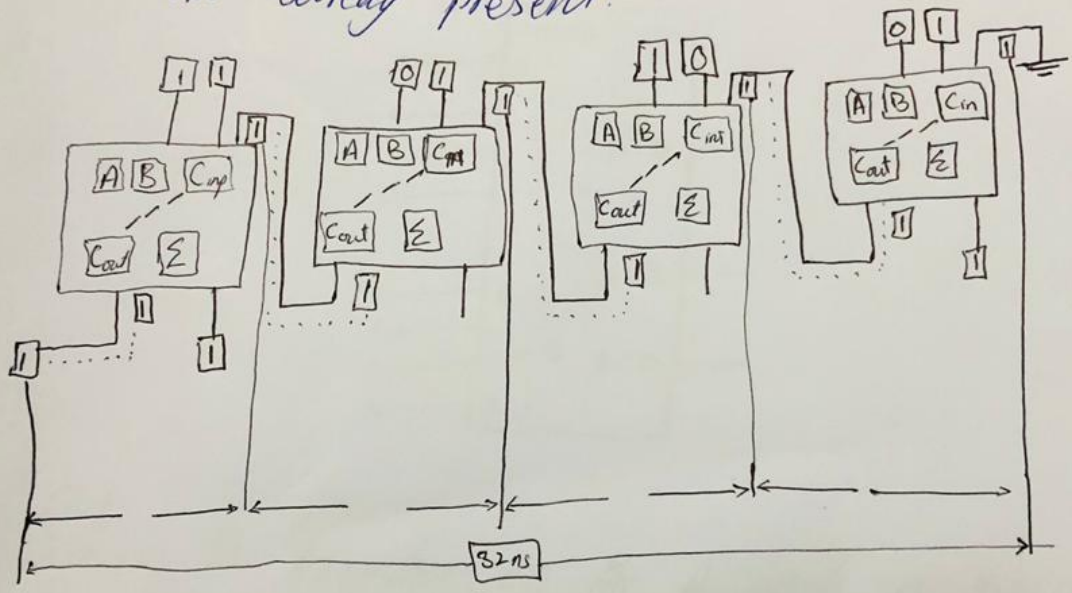
Full adder is the time form the application of the input carry until the output carry occurs, assuming ~~that~~ that the A and B inputs are alreay present.



The answer is

1001

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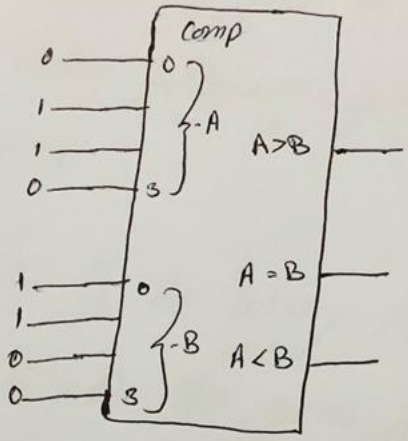
CONo: 04

Determine the A = B, A > B, and A < B output for the input numbers shown on the comparator in figure



Sol: The number on the A inputs is 0110 and the number on the B inputs is 0011 The A > B output is High and the other outputs are Low.

CONO: 05

Show the logic required to convert a 4-bit gray code to binary and use that logic to convert the following gray code words to binary: 1011

Ans: The MSB of the binary number will be equal to the MSB of the given gray code.
Now if the second ~~binary~~ gray bit is 0, then the second binary bit will be the same as the previous or the first bit.
if the gray bit is 1 the second binary bit will alter. if it was 1 it will be 0 and if it was 0 it will be 1.

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The steps is continued for all the bites to do gray code to binary conversion.

Example: Given 1011

gray code to Binary.

$b_3 = g_3 = 1$

$b_2 = b_3 \quad g_3 = 1 \quad 0 = 1$

$b_1 = b_2 \quad g_1 = 1 \quad 1 = 0$

$b_0 = b_1 \quad g_0 = 0 \quad 1 = 1$

Binary code = 1101

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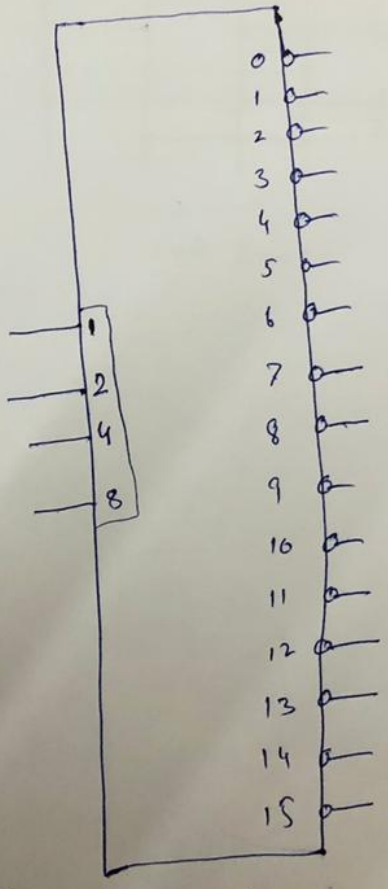
CWO: 06

Draw and explain logic digram for 4-bit active low decoder.

Answer:

5

4 bit Active decoder.



Logic symbol for a 4-line-to-16-line (1 of 16) decoder.

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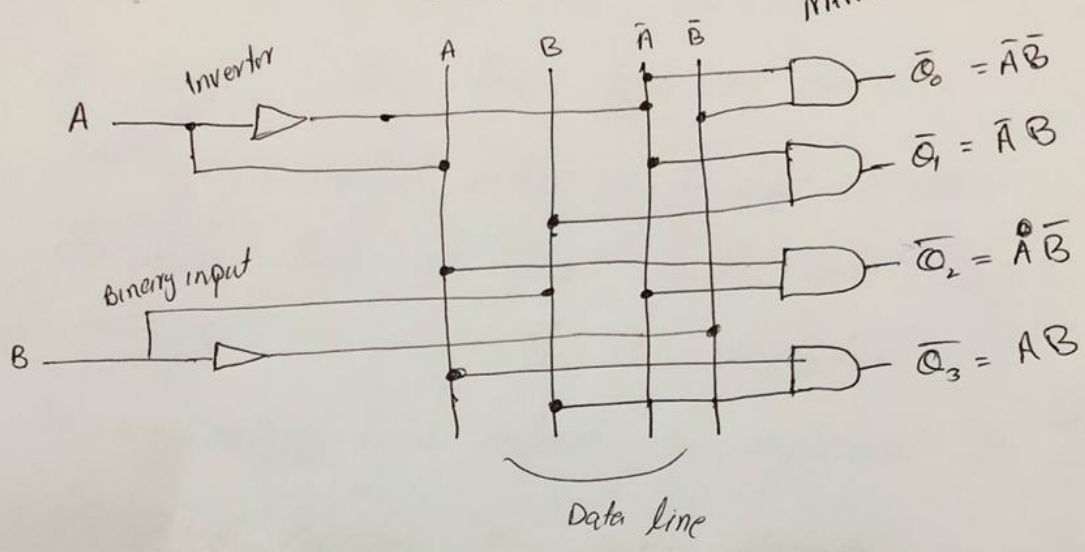
Logic diagram for 4-bit active low decoder.



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the 4 Bit decoder in order to decode all possible combinations of four bites, sixteen decoding gates are = 16. This type of decoder is commonly called either a 4-line decoder because there are four inputs and sixteen outputs or a 1-of-16 decoder.

If an active-Low output is required for each decoded number, the entire decoder can be implemented with NAND gates and inverters in order to decode each of the sixteen binary codes, Sixteen NAND gates are required.

A logic Symbol for a 4-line-to-16 line decoder with active low outputs is shaw in the diagram The BIN/DEC label indicates that a binary inputs makes the corresponding decimal output active.

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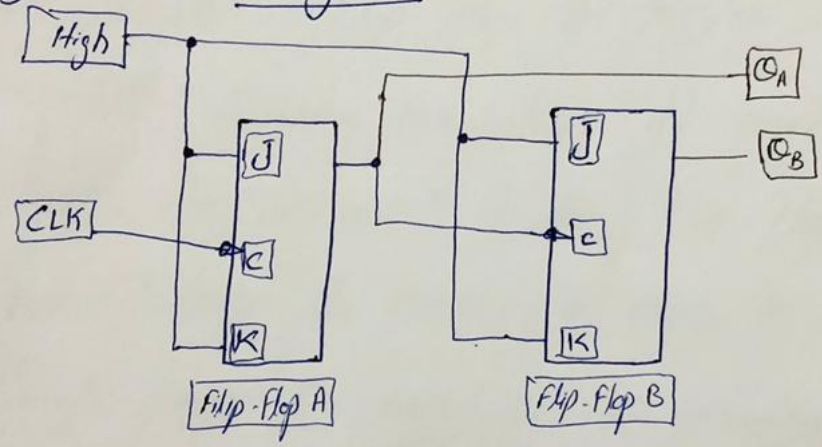
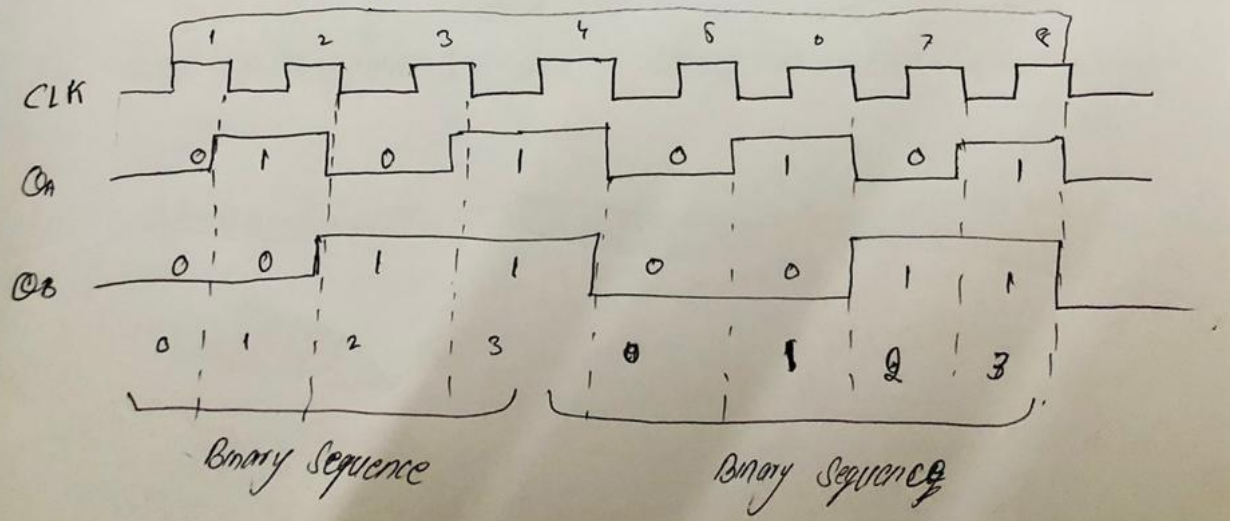
Q 07

Draw and explain the logic diagram for frequency diver (Use 3 J-K flip-flops) and assum 16 khz frequency of the initial wave-form.

Ans:

Diagram





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The logic diagram frequency divider using 3 J-K flip-flop and assume 16 kHz frequency of the intial wave-from. The negative edge triggered J-K flip-flop are used for illustration. Both flip-flop are RESET. Flip-flop A toggles on the negative-going transition of each clock pluse. The Q output of the flip-flop B, so each time Q_A makes a high-to-low transition flip-flop B toggles. The resulting Q_A and Q_B waveforms are shaw in the diagram.

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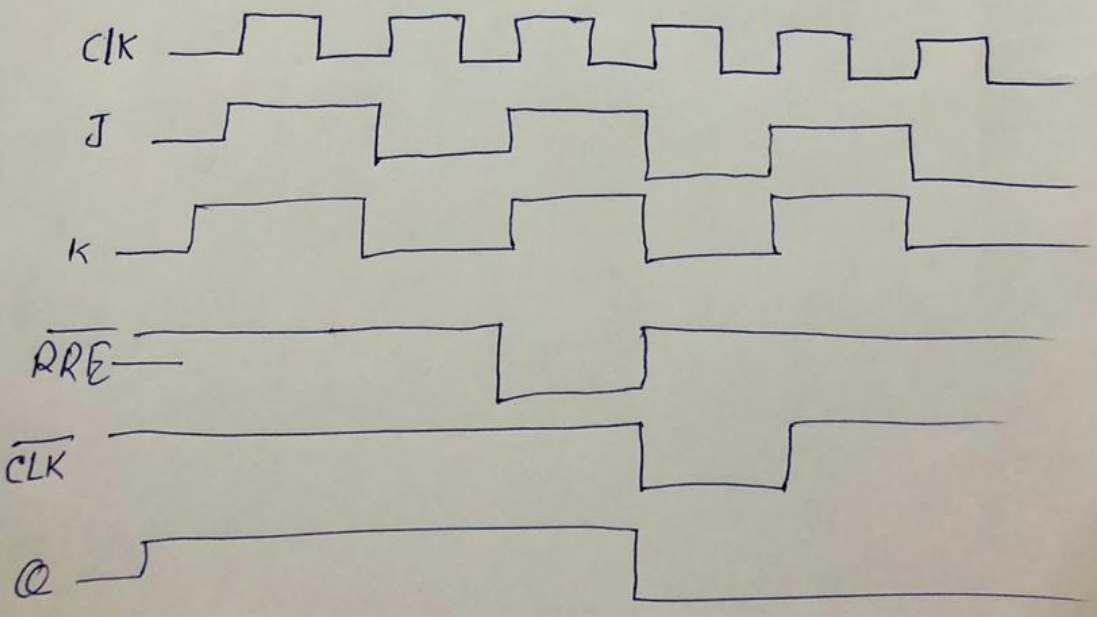
CONO: 08

Determine the Q waveform relative to clock if the signals shown in the figure 04 are applied to the input of the J-K flip-flop. Assume that Q is initially Low

figure 04

Sol:



Q No: 09

Draw the logic diagram and timing diagram for the 4-stage synchronous binary counter.

Sol:

Diagrams

Four bit synchronous counter.