Department of Electrical Engineering

Assignment

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Course details

Course title: VLSI

Module: 6th

Student details

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Part A (objective type)

1) In cmos circuit which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance?

a) Static dissipation
✓2) Dynamic dissipation
3) Both and B
4) none of these above.

2) which type of MOSFETs Exhibits no current at zero gate voltage?

*) Depletion MOSFET
✓2) Enhancement MOSFET
3) Both a & b
4) None of these. above.

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3) CMOS circuit are constructed in such a way that all PMOS transistor must have either an input from the voltage source or from another

a) pmos transistor
2) cmos transistor
3) cmos transistor
4) BJT transistor

4) Delay which is equal to the time taken by a gate output transistor. to 0, from another value 1, x, or z is.

1) Rise delay
2) fall delay
3) turn off delay
4) turn on delay

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5) which type of simulation model is used to check the timing performance of a design?

1) transistor level
2) Gate level
3) Behavioral
4) Switch level
5) none of these.

6) which of the following statements is incorrect.

a) some PLDs are programmed using electrically operated switches.

2) Some PLDs are programmed using mechanically switches.

(Pg 4)

Fill in the blanks

7) In MOS devices, the current at any instant of time is constant/independent of the voltage across their terminals.

8) For complex gate design in CMOS, or function needs to be implemented by connections of MOS.

a) Parallel

9) In the following DIA, which output implements the logic function $\overline{ABCD}$?

- X
- Y
- Z ✓

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10) The term VLSI means a device containing between thousand and million transistors.

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Part B (Subjective type)

Q.1) In low power VLSI design clockgating technique will reduce power all time or it depends upon the input data? is any change, the computation power may increase?

Ans) Using this clock gating technique the flip-flop clocks only when the output req to change. Clearly this means that the FLop will clock less in the circuit then in the Previous one. in reality when this is done via the synthesis tool, rather than just an "and" gate, a latch (integrated)

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cell in the library is used with the "and" to prevent glitch issues when the timing of the clock and enable are different clock-tree synthesis, there may also be added observability for DFT regions.

Clearly, a gating structure would not be applied to every register since the cost in the power of the gating would exceed the saving on a flop.

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Q No 2

if we want to design an IC and I want that each every transistor used in this IC should be Optimized individually with less time. How it will be possible??

(Ans)

Integrated circuit design:-

IC design, is a subset of electronics engineering, encompassing, the particular logic and circuit design techniques required to design Integrated circuits, or ICs, ICs. consist of miniaturized electronic components built into an electrical network on a monolithic semiconductor substrate by photolithography.

IC design can be divided into the broad categories!

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Analog :-

Analog IC design is used in the design of op-amps, Linear regulato Phase locked loops, oscillatory and active filters Analog design is more concerned with the Physics of the semiconductor devices, such as gain matching, power dissipation, and resistance. Fidelity of analog signal amplification and filtering is usually critical and as a result.

- analog ICs. use larger area active devices.

Digital. Digital IC design is to produce components such as micro processors, FPGAs, memories (RAM, Rom) and digital ASICs, Digital focus on logical correctness maximizing circuit.

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~~Design~~ Densing, and Placing circuit so that clock and timing signals are routed efficiently - Analog IC design also has specialization in power IC design and RF IC design.

- digital designs and are usually less dense in circuitry.

transistor are used in every IC!

the number OF transistor is used in every IC started to increase exponentially in fact, in 2006, chips were created that contained up to 100 million transistors per square centimeter.

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It can be possible!

Integrated circuits are found every technological device that we use today from computers and calculators to watches and cellular phones. An integrated circuit (IC) is a tiny silicon chip, less than a centimeter in width. Among other thing, the IC contains arrays of transistors that help process data. The more transistor there are in a circuit the faster the data is processed. Modern technology has allowed data to be processed rapidly by increasing the number of transistor and decreasing the size of the IC.

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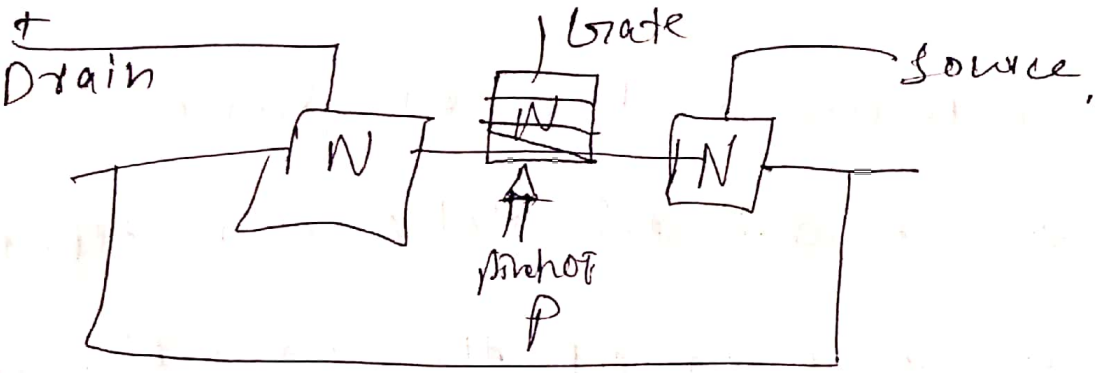
Q No 2 / b

NMOS or PMOS Fabrication Process

There are a huge number and assorted of fundamental fabrication steps utilized as a part of the generation of present-day MOS ICs, A similar procedure can be utilized for the planned of NMOS or PMOS CMOS devices, the most commonly used material could be either metal or poly-silicon- the most a strategic distance from the nearness of parasitic transistor various are acquired the system that are utilized to isolated the devices in the wafer. the NMOS

Fabrication steps are as per the following.

NMOS Fabrication Process



NMOS Fabrication Steps

Using the fundamental processing steps, OF the Poly-Sigate self-aligning nmos technology are discussed below it can be superior understood by allowing for the fabrication OF a single enchancment-type transistor. the step by step procedure OF NMOS Fabriation steps include the following

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Step 3!

The exterior (surface) is now enclosed with the photo oppose which is deposit onto the wafer and spun to an even distribution of the necessary thickness.

Step 4!

The photoresist coating is then uncovered to ultraviolet (UV) light through masking which describes those areas into which transmission is to take place as one with transistor channels. Suppose, for example, that areas uncovered to UV radiations are polymerized, but that the areas necessary for diffusion are protected by the cover and remain unchanged.

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Step 5!

These regions are consequently readily fixed away together with the original silicon-di-oxide so that the surface of the wafer is uncovered in the window defined by the mask.

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(Q3) Draw a stick diagram of a Layout using that variable ordering

$F = ACD + ABD$

Ans)

Stick Diagram:

* Stick diagrams help plan layout quickly
  - need not be to scale
  - Draw with color.

*Sketch a stick diagram for $(A+B+C)\cdot D$