Lab 10: Shift Register

DIGITAL LOGIC DESIGN

Submitted to :

Sir.Muhammad Amin

Submitted by :

Muhammad Hamza

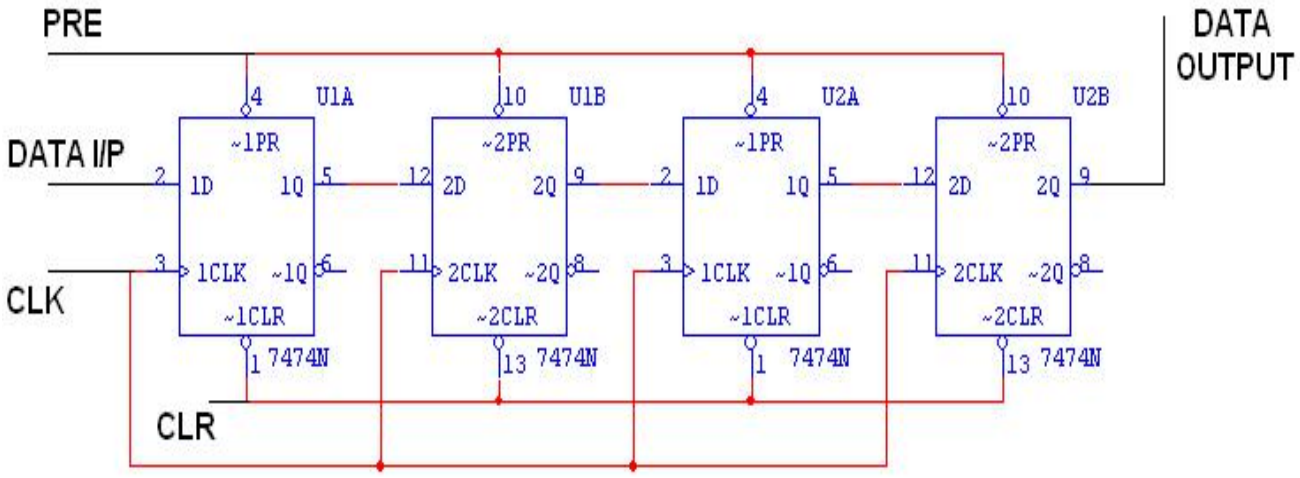
ID = 13136

BS (SE) Section B (8th semester)

To Design and verify the function of Truth Table Observation Table:

Objective: • To investigate the operation of the shift registers

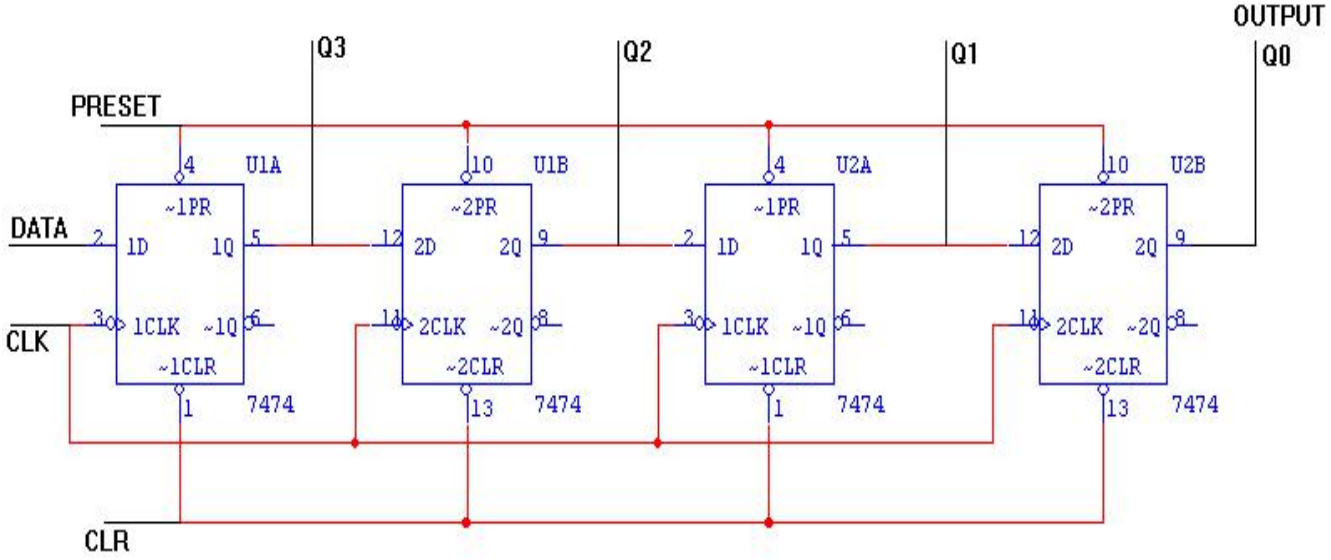
SERIAL IN SERIAL OUT:



Truth Table for SERIAL IN SERIAL OUT:

CLK	Serial in	Serial out
1	1	0
2	0	0
3	0	0
4	1	1
5	x	0
6	x	0
7	x	1

SERIAL IN PARALLEL OUT:

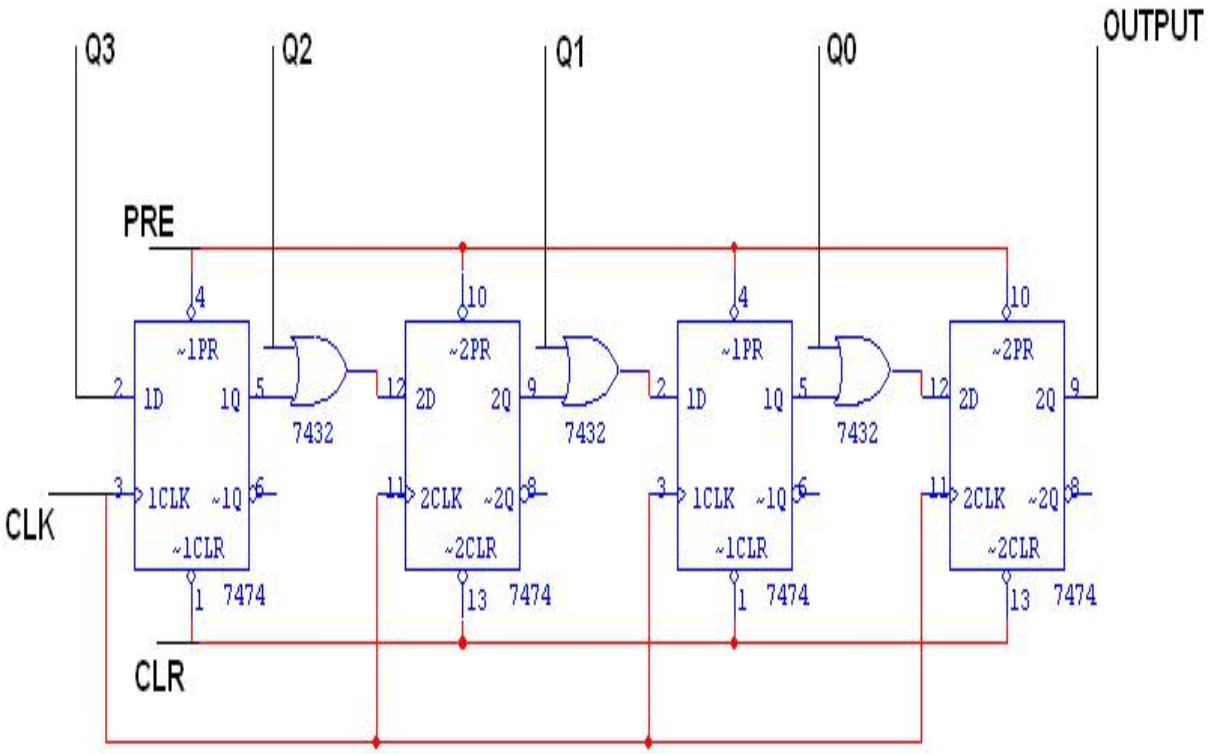


Truth Table for SERIAL IN PARALLEL OUT:

OUTPUT

CLK	*DATA*	Q_A	Q_B	Q_C	Q_D
1	**1**	**1**	**0**	**0**	**0**
2	**0**	**0**	**1**	**0**	**0**
3	**0**	**0**	**0**	**1**	**1**
4	**1**	**1**	**0**	**0**	**1**

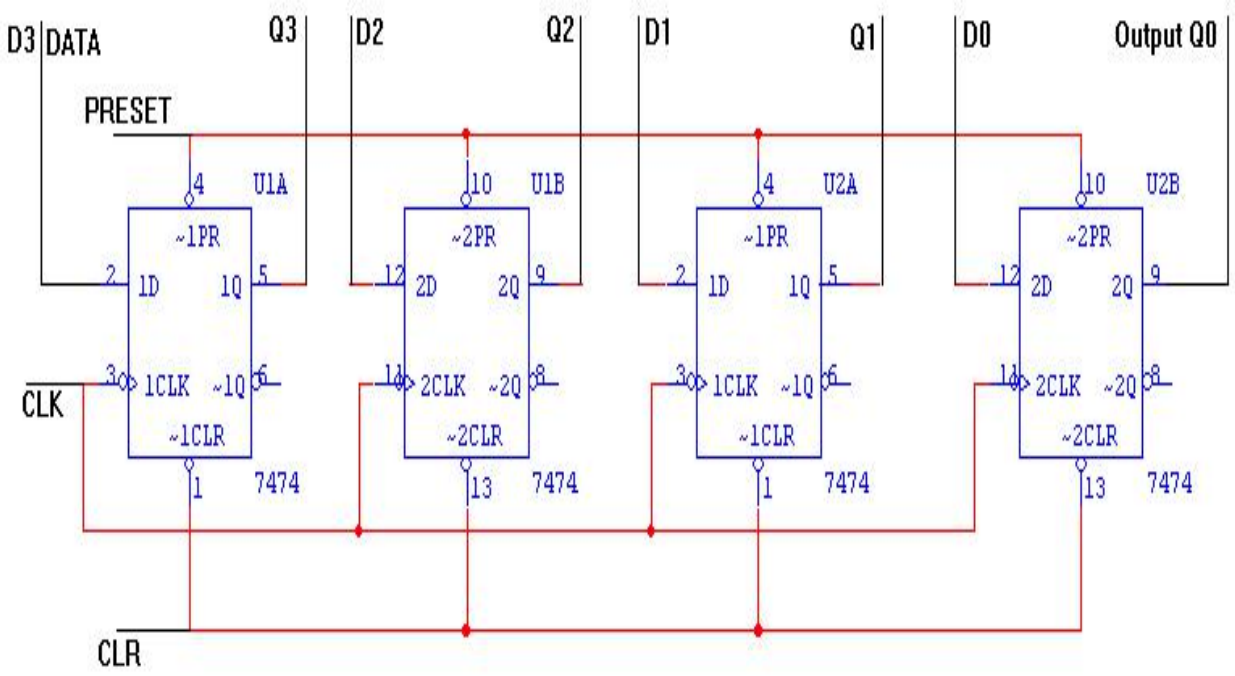
PARALLEL IN SERIAL OUT:



Truth Table for PARALLEL IN SERIAL OUT:

CLK	Q3	Q2	Q1	QO	O/P
0	**1**	**0**	**0**	**1**	**1**
1	**0**	**0**	**0**	**0**	**0**
2	**0**	**0**	**0**	**0**	**0**
3	**0**	**0**	**0**	**0**	**1**

PARALLEL IN PARALLEL OUT:



Truth table for PARALLEL IN PARALLEL OUT:

CLK	DATA INPUT				OUTPUT			
	DA	DB	DC	DD	QA	QB	QC	QD
1	1	0	0	1	1	0	0	1
2	1	0	1	0	1	0	1	0