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DeP:: BScs
Subject: Basic Electronics
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(Q NO: 1)

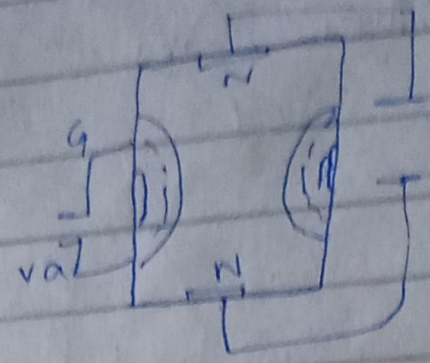
(A) Explain JFET works including the Pinch off and course cutoff voltage ?

Ans/

The working of JFET can be explained as follows.

Case I

When a voltage V_{DS} is applied between and Source voltag Terminals and voltage on the gate is zero as shown in the following figure. The two pn function at the sides of the BAR establish depletion layer.



And the cut off voltage is voltage at which a battery is considered fully discharged could cause harm and the Pinch off voltage is the drain to source voltage after which the drain source current becomes almost constant and JFET enter into saturation region. and is defined only when gate to source is zero.

Compare the JFET and bipolar Junction transistor. Also explain the advantage and disadvantage of each.

Ans: The comparison of the JFET and bipolar junction transistor. Also explain the advantage and disadvantage of:

is reverse biased the gate current is particularly zero.

And the base current of the BJT is always some value greater then zero.

Advantage of JFET.

i) The JFET has high input impendem

ii) JEET are protected to radiation

iii) The JEET is a low Power Consumption device.

Disadvantage.

i) The main disadvantage of JFET is relatively low gain bandwith product.

2) The performance of JEET go down as frequency increases due to feedback by internal capacitance.

Advantage of BJT:

1) It has a large gain band with.

2) It shows better Performance at high frequency.

3) It has a better voltage gain:

Disadvantage.

i) The BJT is more can effect of radiation.

ii) It more noia Produced.

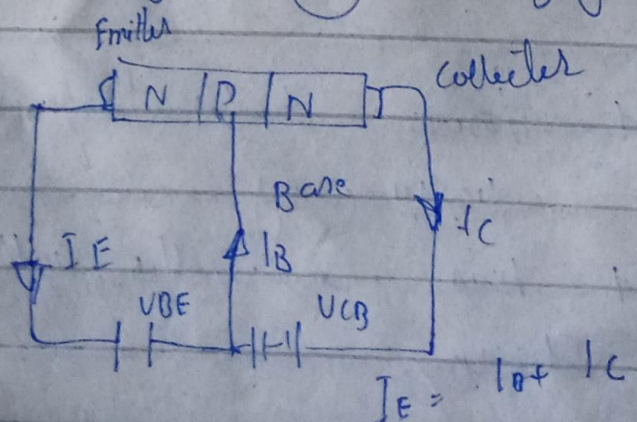
iii) It has a low thermal stability.

Q. NO: 2.

a) Draw a npn. transistor showing the P region. And the bias transistor properly and explain how it works?

Bipolar transistor or BJT comes in to basic forms. And NPN negative - positive Negative and PNP. (positive Negative

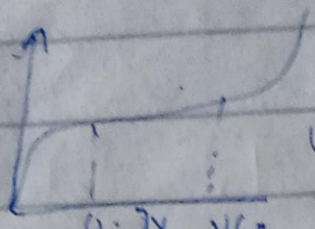
The most commonly used transistor is NPN. A bipolar NPN transistor configration drown following configration.



$I_E = I_B + I_C$

(6).

A graph of the collector characteristics Ic verses Vce is shown in following fig.

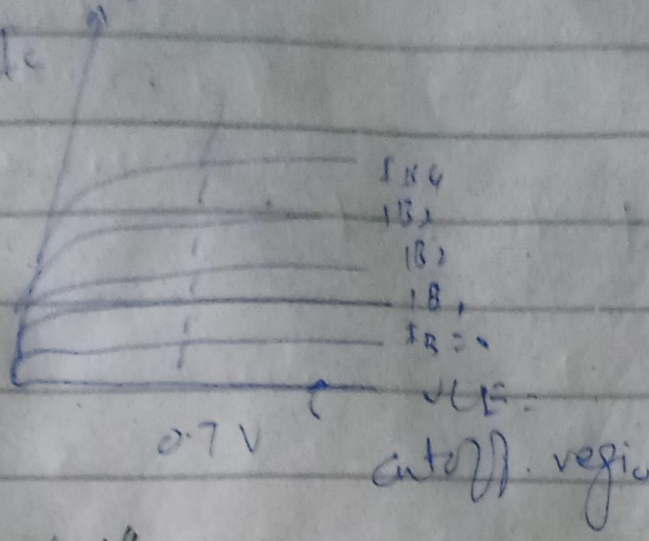


Suppose VBB and Vcc are produce a current $i_B = 0$ and $V_{CE} = 0V$ then both BE and BC function are forward biased. The saturation region corresponds to the case where both both function are forward biased.

if Vcc increases to much the transistor goes into the breakdown region. This should be avoided.

The following fig. shows collector Curves for different four values of base current when $I_B = 0$ the transistor is in its cutoff region. and only a small leakage.

Current flows as I_C

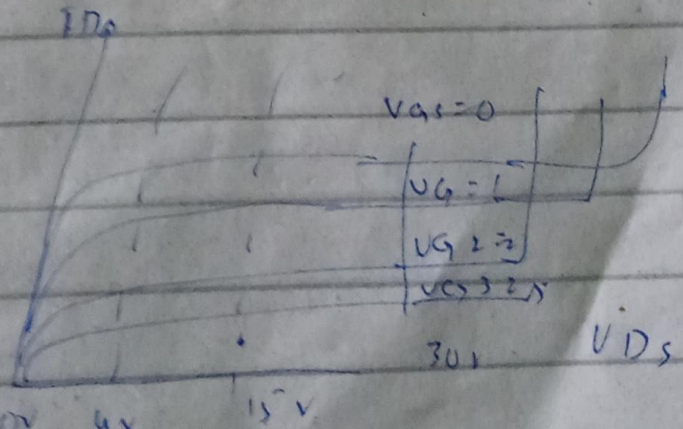


Q:NO:1

b)

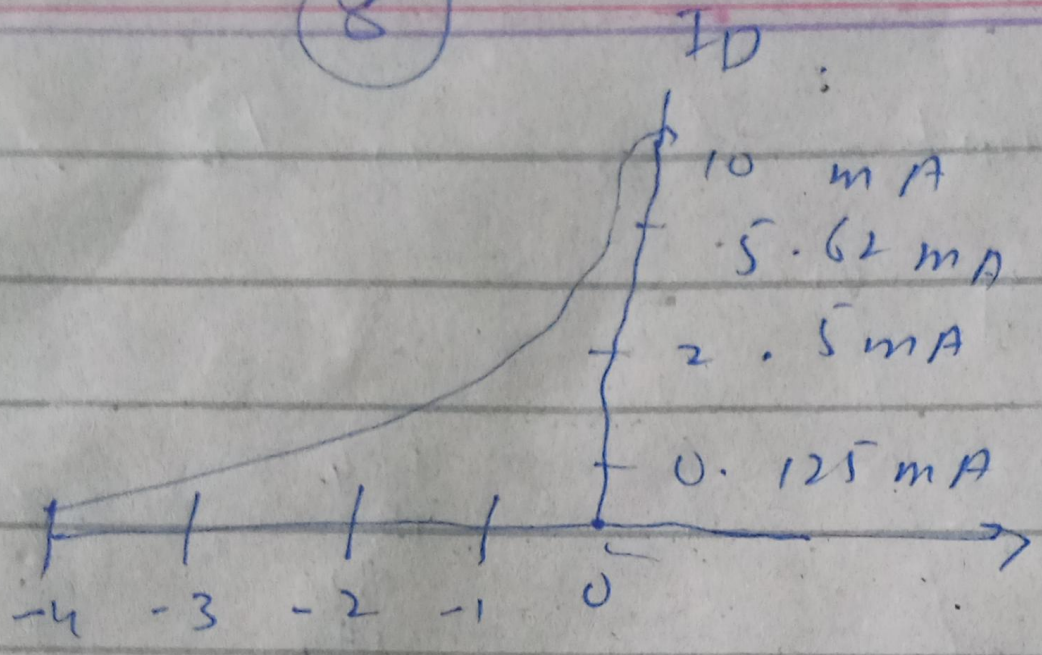
Draw the drain curves and the tran Conditions Curve for a JFET?

Ans. The following are the drain curves and the trans Conduction Curve of a JFET.



(a) (Drain Curves

(8)



b) Trans conductance curve