Digital Logic Design

Assignment 6
Sir. Muhammad Amin

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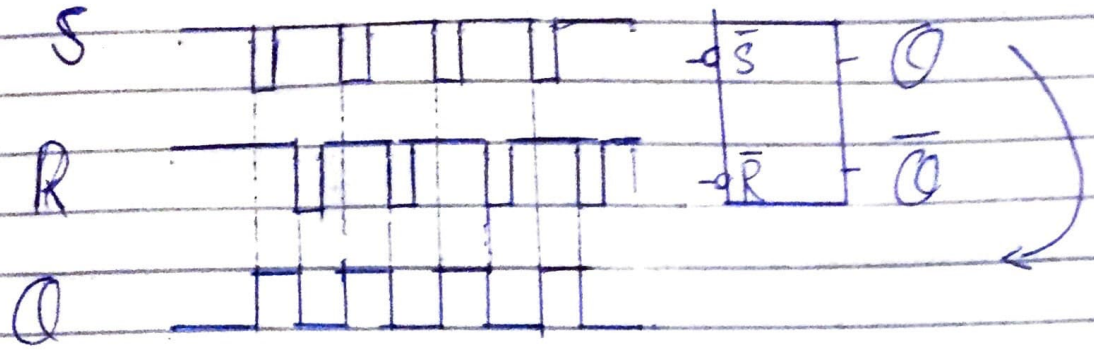
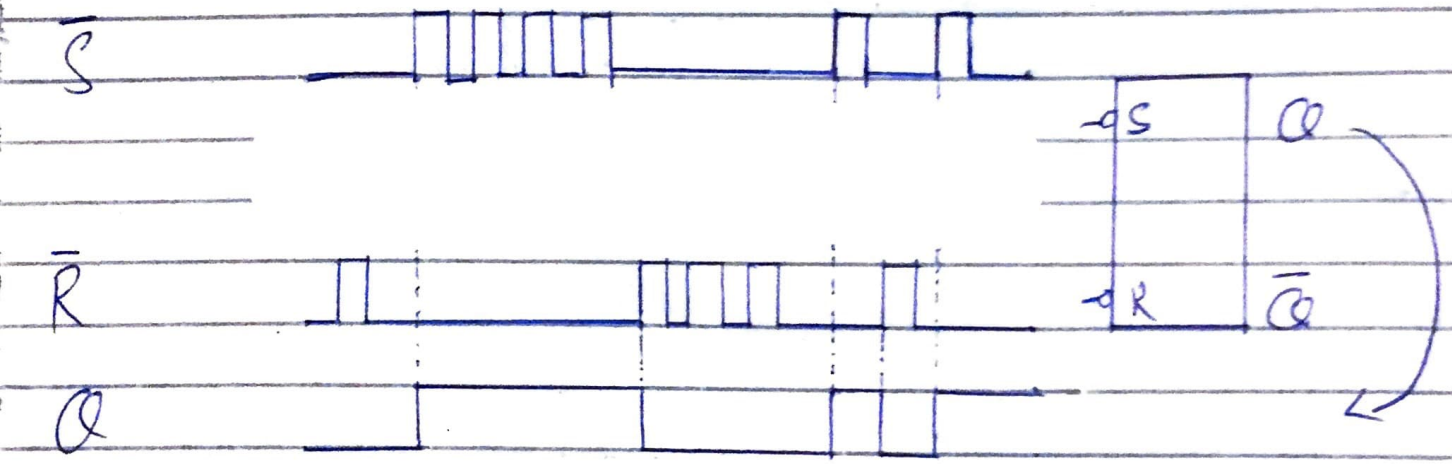
15453
Csc-201

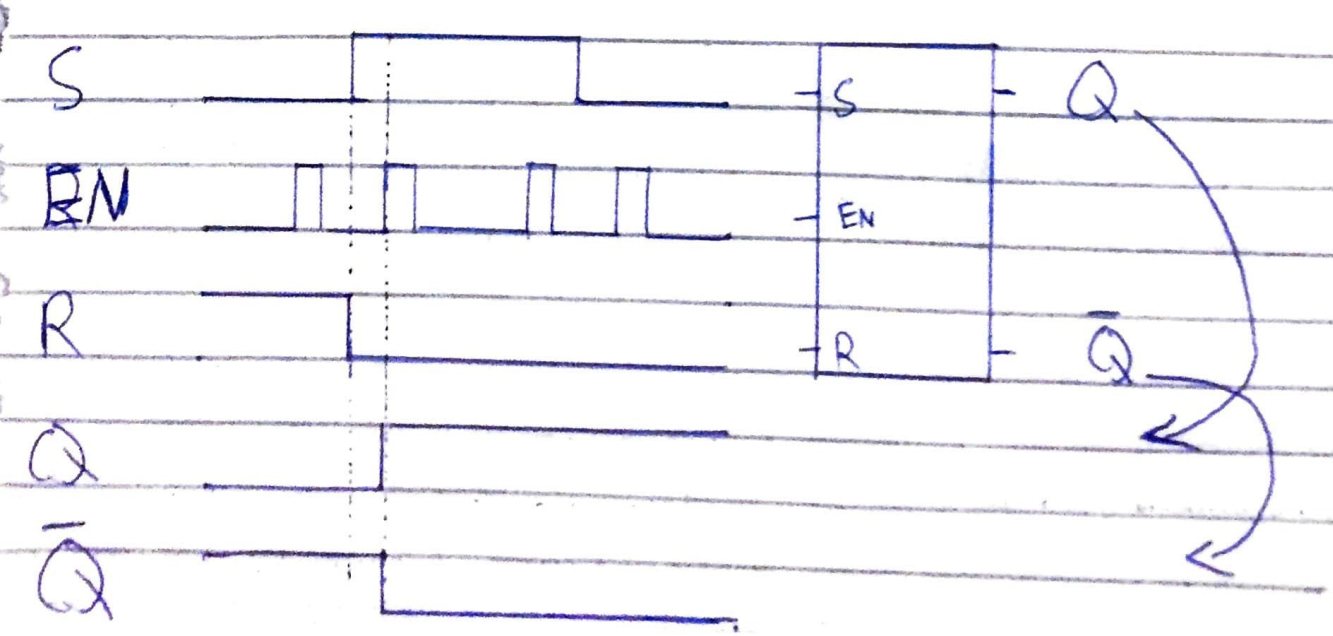
Q1



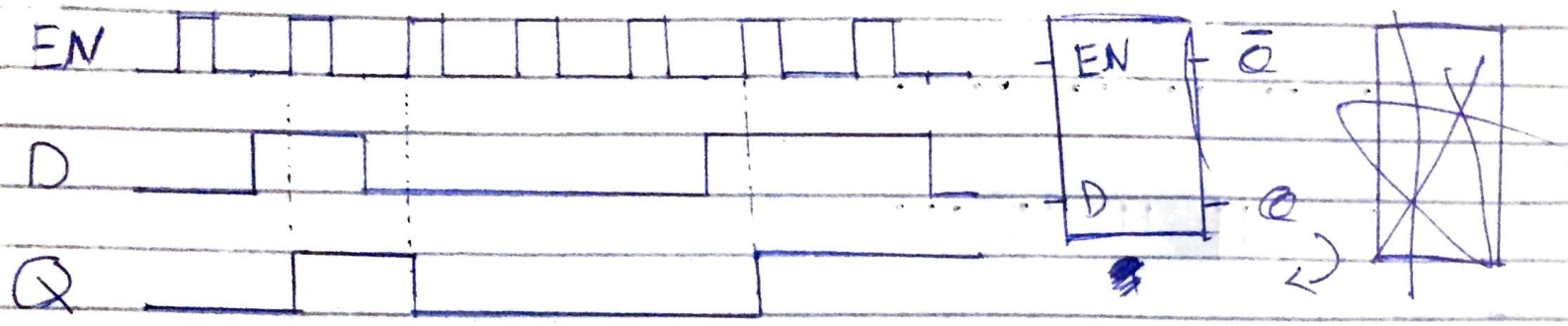
Q2



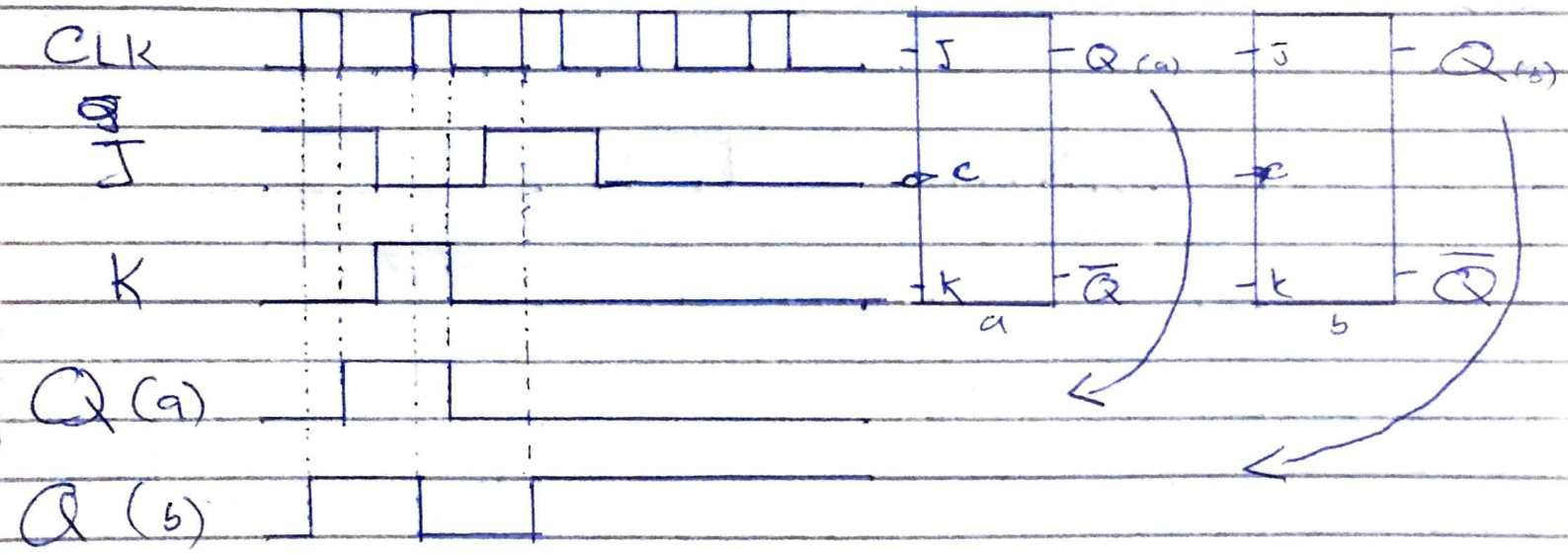
Q3



Q4



Q5

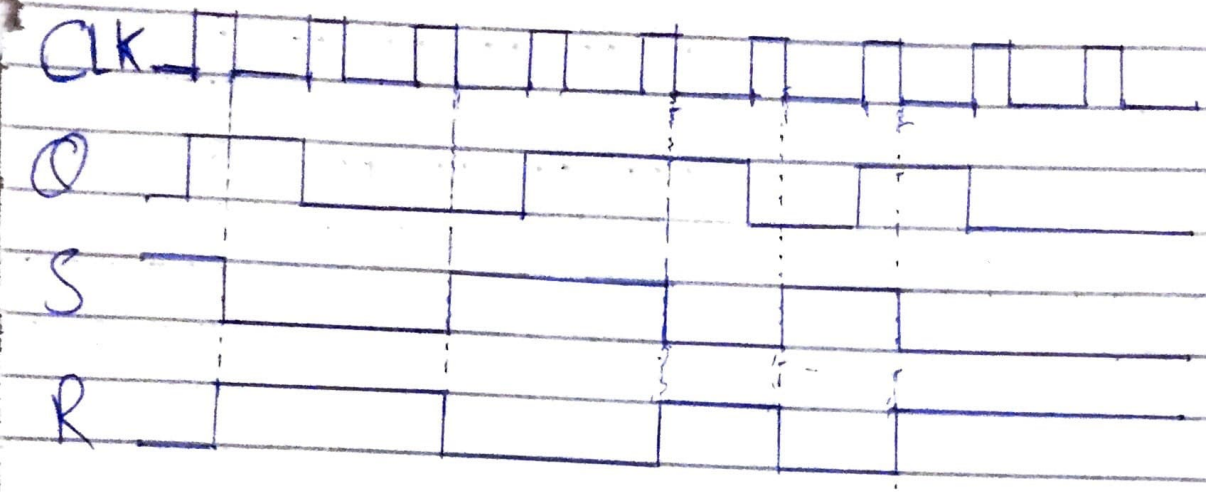


The main difference between (a) and (b) edge triggered JK-Flip-Flops is that

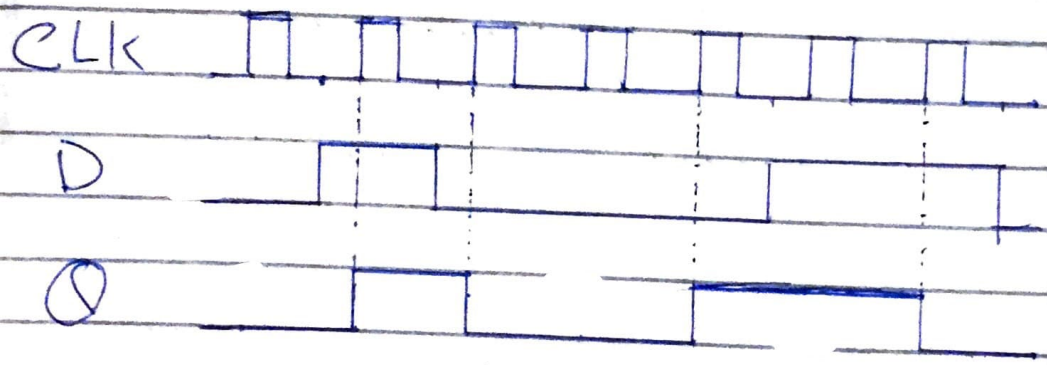
The flip flop (a) triggers on the -Negative edge of the clock pulse, while

The flip flop (b) triggers on the +Positive edge of the clock pulse.

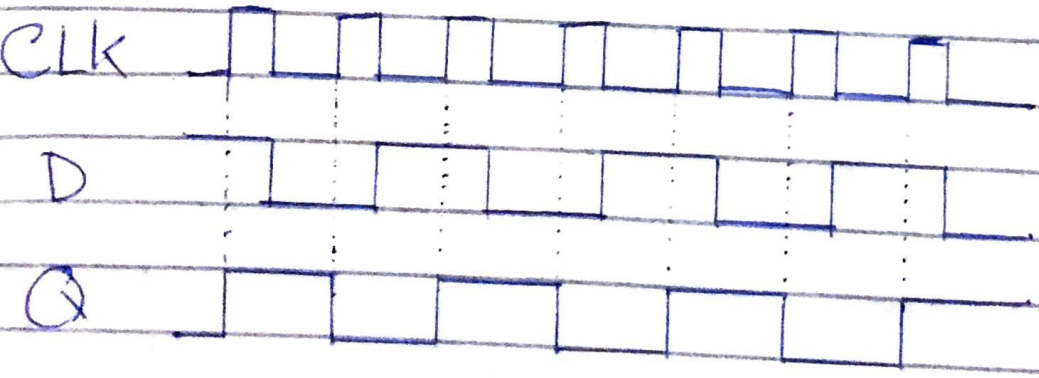
(b)



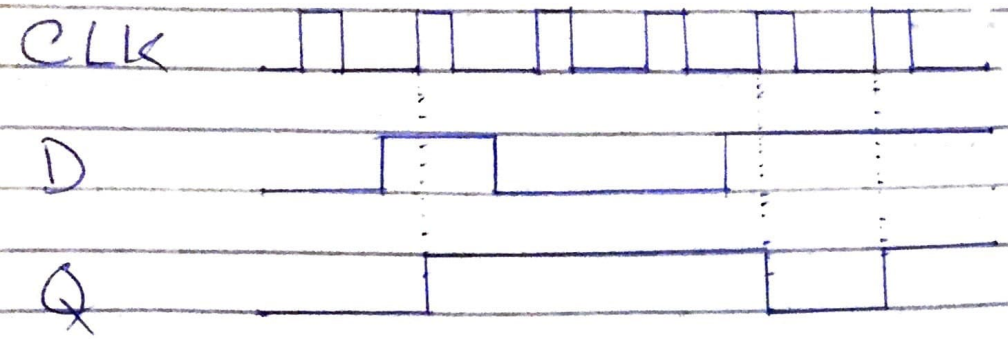
Q7:



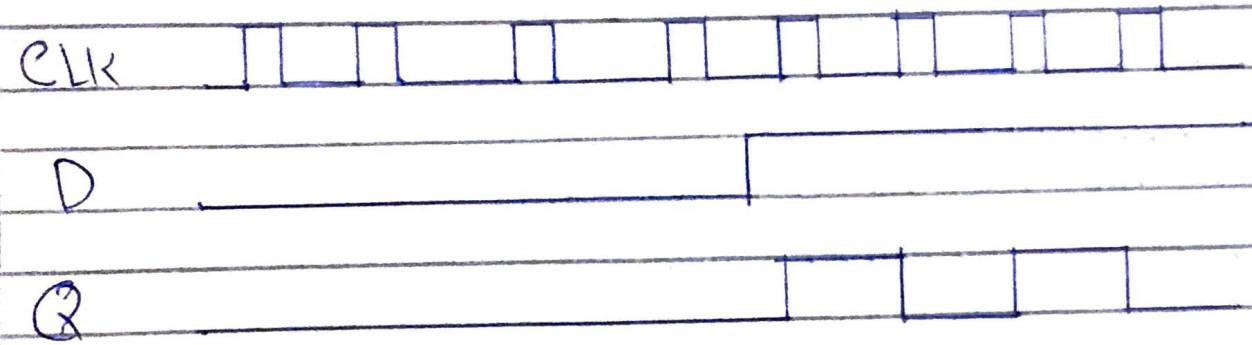
Q8:



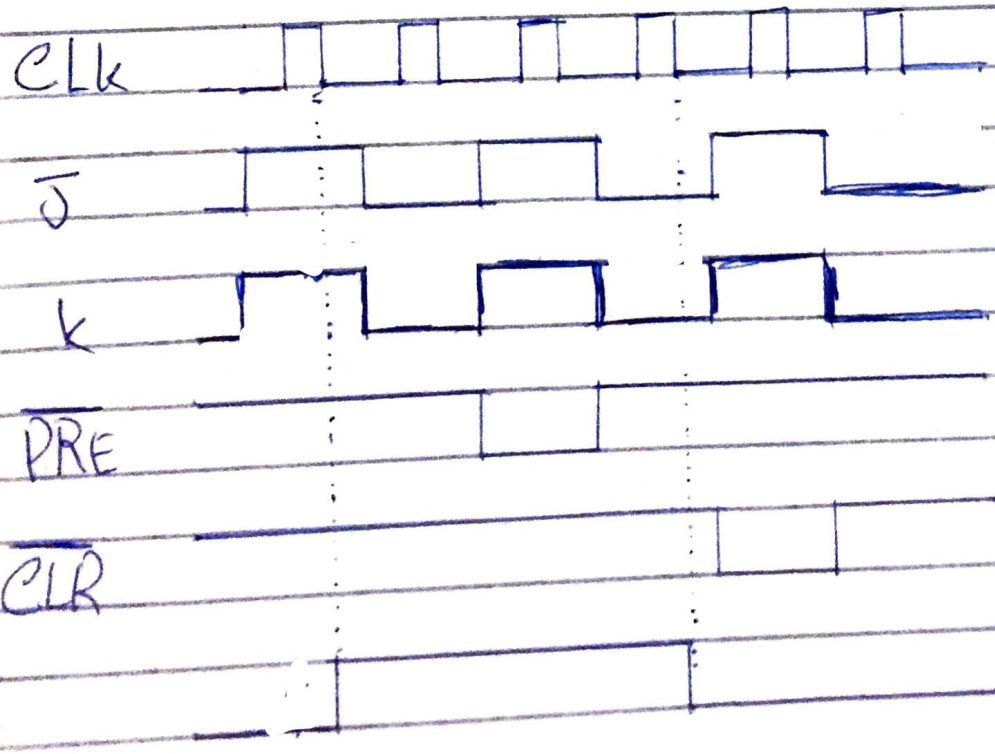
Q9:



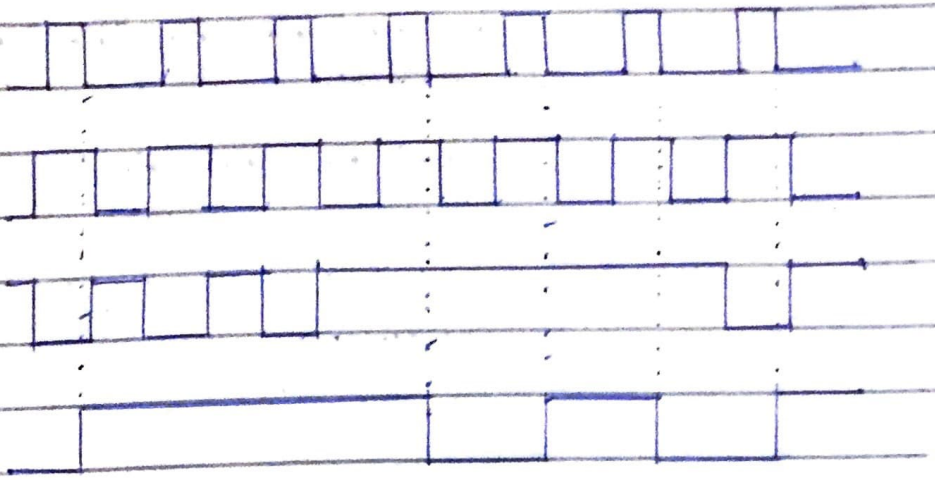
Q10:



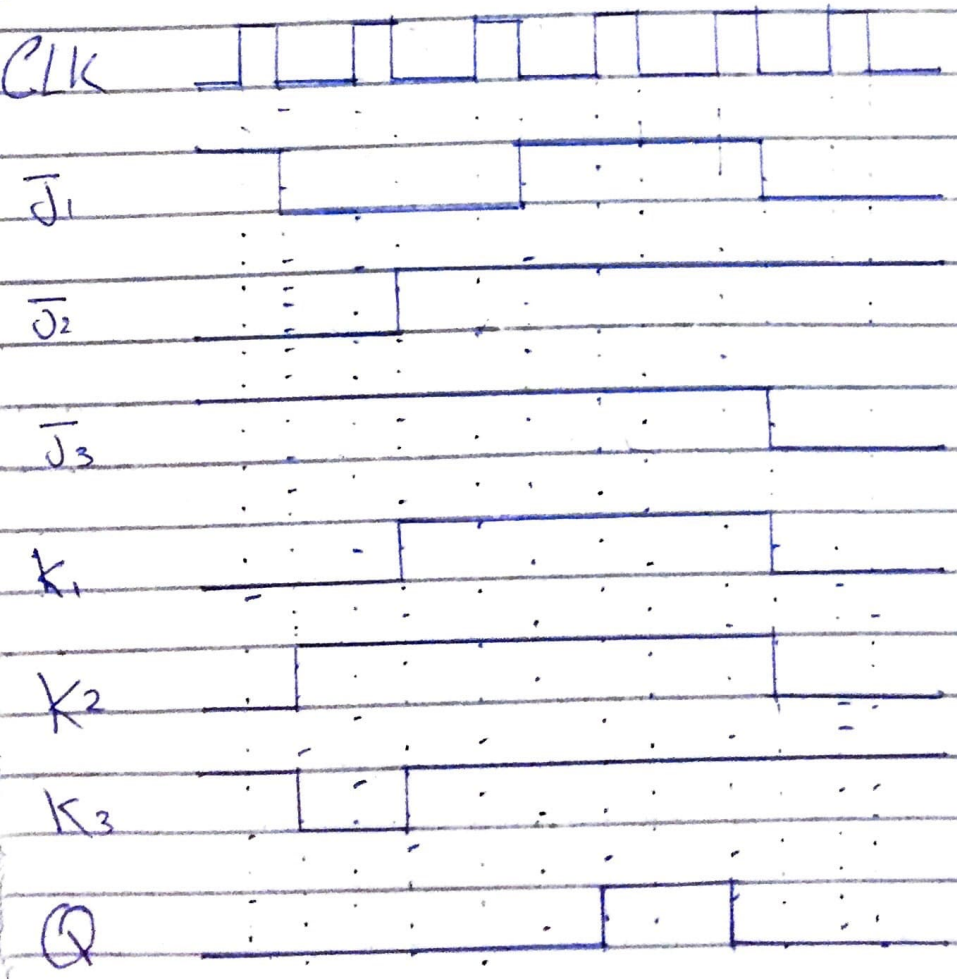
Q11:



Q12



Q13 14



Q#13

$\bar{J}_1 = 10100011$

$\bar{J}_2 = 01110101$

$\bar{J}_3 = 11110000$

$\bar{J} = 00100000$

$K_1 = 00011101$

$K_2 = 11010100$

$K_3 = 10101011$

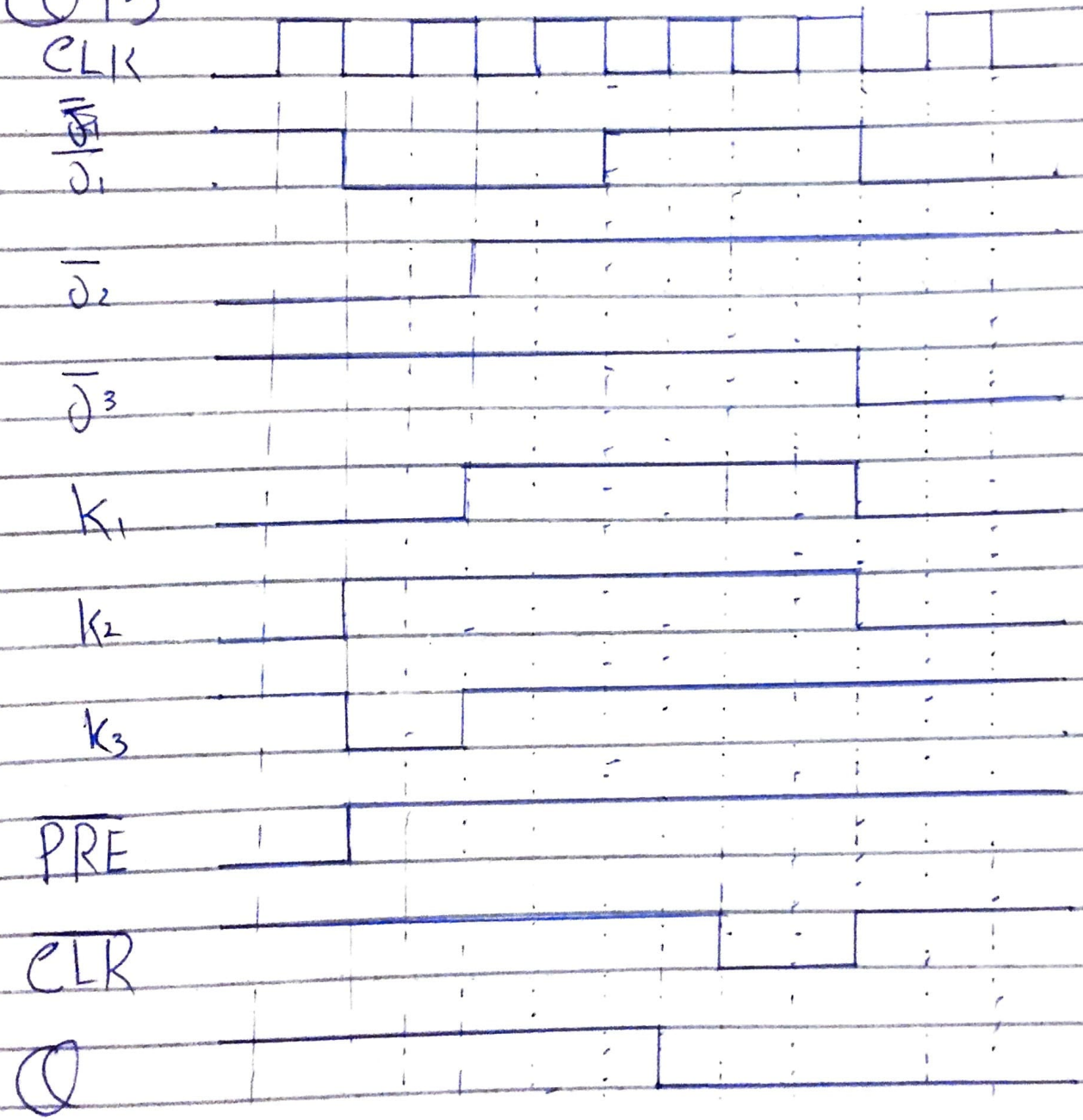
$K = 00001000$

$\bar{Q} = 00100000$

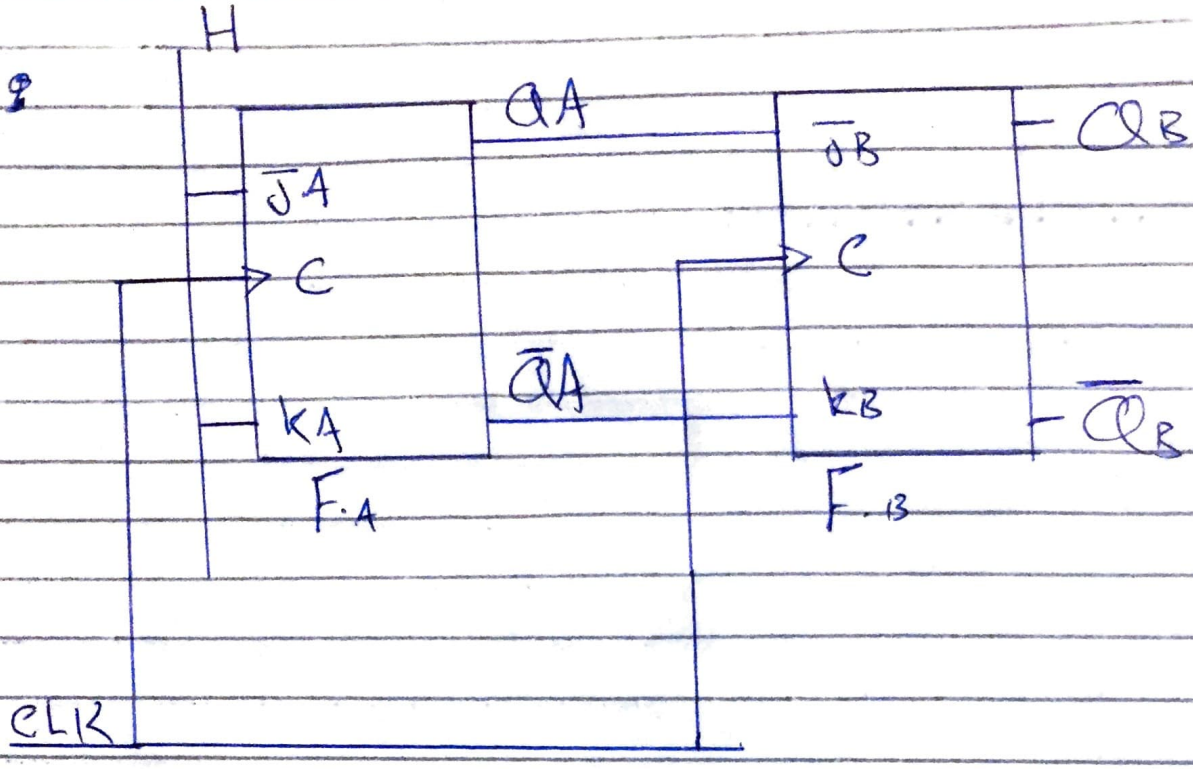
$K = 00001000$

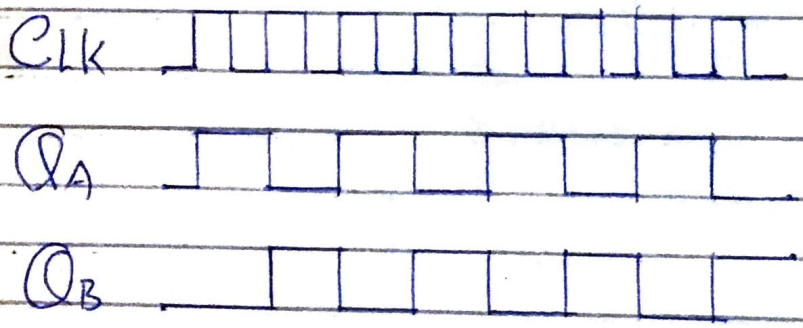
$Q = 00110000$

Q15

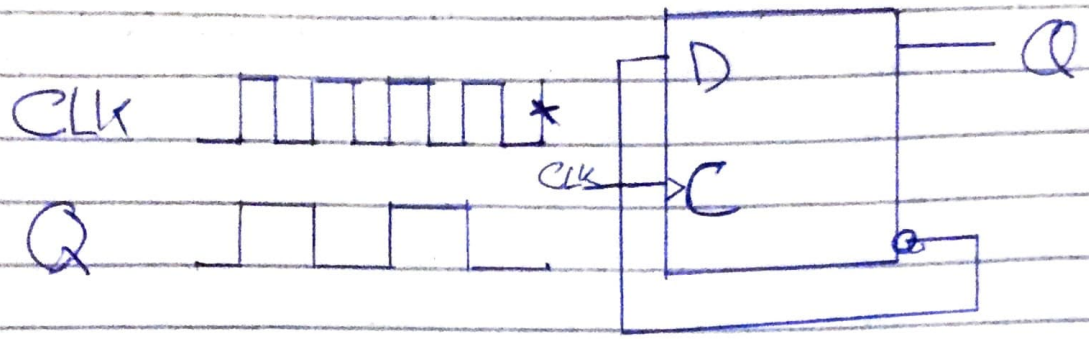

CLK
$\overline{J_1}$
J_1
$\overline{J_2}$
$\overline{J_3}$
K_1
K_2
K_3
$\overline{PRE}$
$\overline{CLR}$
Q

Q6 H



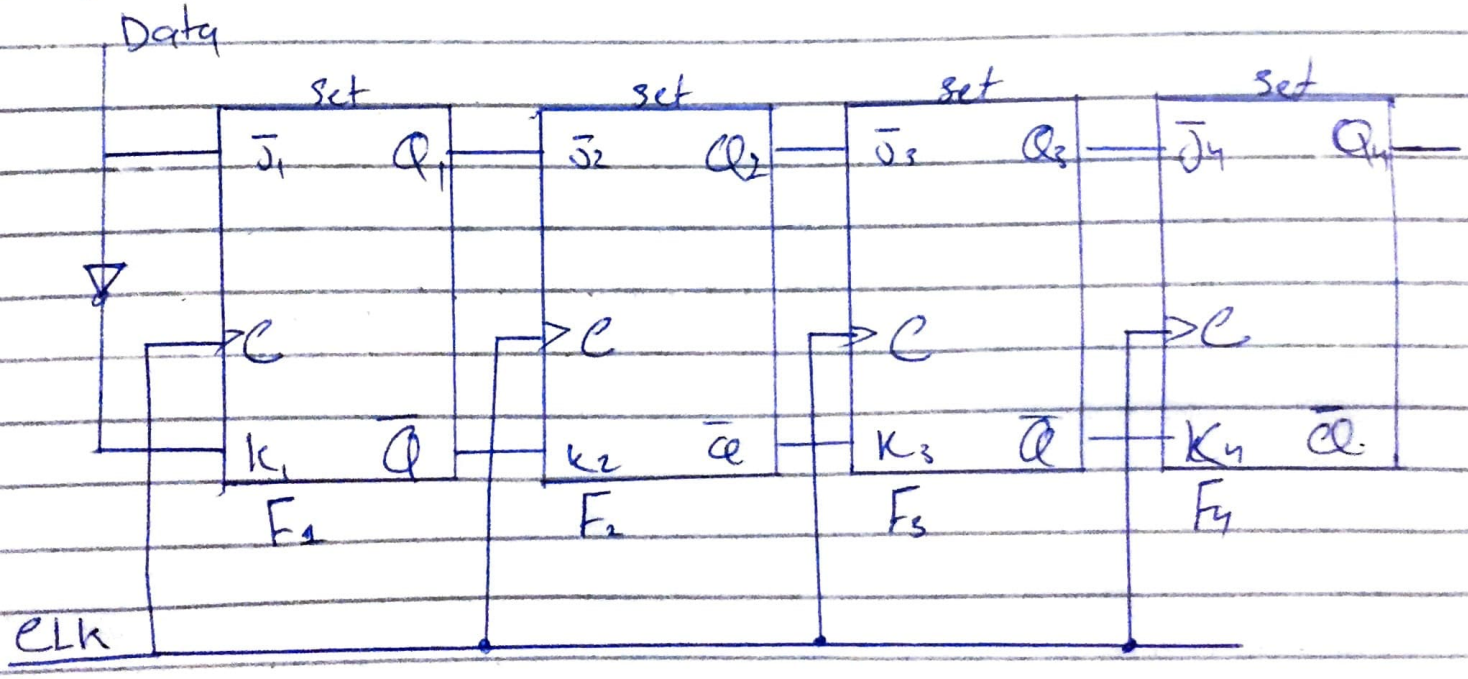


Q17:

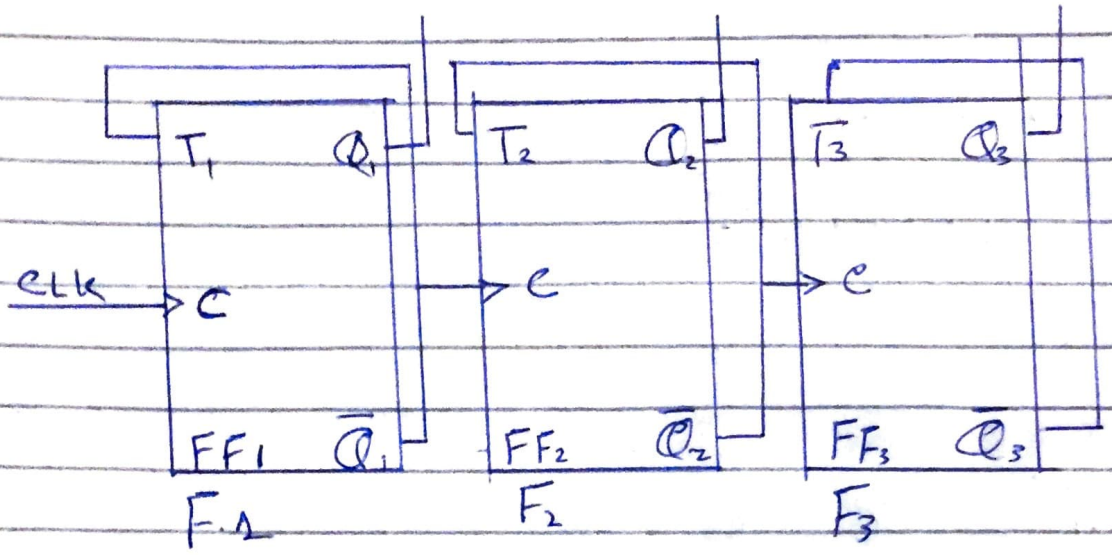


The device performs the Divide-by-two function

Q18:



Q19: $Q_A = f/2$ $Q_B = f/4$ $Q_C = f/8$



Here if the input frequency is 8 kH then at given nodes frequency will be as follows

$Q_A = f/2 = 4$ kh

$Q_B = f/4 = 2$ kh

$Q_C = f/8 = 1$ kh