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ANS: The type of exchange that are needed by indicating the major forms of input & output for processor, memory & I/O modules are;

* Memory to processor:-
  The processor read that INSTRUCTION or a unit of data from memory.

* Processor to memory:
  The processor write a unit of data to memory.

* I/O to processor:
  The process read data from I/O device via an I/O module.

* Processor to I/O
  The processor send data to the I/O device.

* I/O to or from memory:-
  From these two cases an I/O modules is allow to exchange data directly with memory, without going through the processor, using direct memory access.

performed & operand(s) to be used.

* Operand address calculation (OAC):-
  if the operation invoke reference to an operand in memory or available via I/O then determine the address of the operand

Operand fetch (OF):-
  Fetch the operand from memory or read it in form I/O

Data operation (DO):-
  Perform the operation indicated in the instruction

Operand store (OS)
  Write the result into memory or out to I/O.

C:- Classes of interupts:-

  its generated by some condition that occur as a result of an instruction execution such as arthimatic overflow, division by zero, attempt to execute an illegal machine instruction, or reference outside a user's allowed memory space.

* Timer:-
  its generated by a timer within a processor. This allows the operating system to perform certain function on a regular basis.

I/O:-
  its generated by an I/O controller to signal normal completion of an operation request service from the processor, or to signal a variety of error condition.

D:- BUS interconnection Scheme:-
The most common computer interconnection structure are based on the use of one or more system buses.

* A system bus consists, typically of from about fifty to hundreds of seprate lines. The lines can be classified into three functional groups, data, address, & control lines

* Data lines:-
The data lines provide a path for moving data among system module These lines collectively are called the data bus.

* Address lines:-
The address lines are used to designate the source of destination of the data on the data bus. The width of the address bus determines the maximum possible memory capcity of the system

* control lines:-
The control lines are used to control the access to & the used of the data & address lines. Because the address & the data lines are shared by all components, there must be a means of controling their use. Typical control lines include. Memory write, memory read, I/O write, I/O read, transfer ACK, Bus Request, Bus grant, interupt Request, interupt ACK, clock & reset.

Q3:- Differentiate each of the following:-

A:: Programing in hardware & programing in Software.

* programing in hardware:-

The program is in the form of hardware & term a hardware program. Suppose we construct a general purpose configuration of arthmatic & logic function this set of hardware will perform various function on data depending on control signals applied to the hardware. In orginal case of customized hardware the system accept data & produce result.

* programing in Software:-

The new method of programing which is a sequence of codes or instruction is called Software In this method programing is much easier, instead of rewiring the hardware for each new program all we need to do is provide a new sequence of code. each code is in effect an instruction

& part of the hardware interprets each instruction & generates control signals.

B:- program flow of control without interupt & with interupt

Ans: in the interupt cycle, the processor check to see if any interupts have occured, indicated by the presence of interupt signal.

* if no interupt are pending, the processor proceed to the fetch cycle & fetches the next instruction of the cussent program

C:- Disabled interupt & nested interupt processing

A disabled interupt simply means that the processor can & will ignore that interupt request signal. if an interupt occur during this time it generally remain pending & will be checked by the processor after the processor has enabled interupts.

* A nested interrupt is to allow an interrupt of higher priority to cause a lower priority interrupt handler to be itself interrupted. A user program begins at t = 0, At t = 10 a printer interrupt user information is placed on the system stack & execution continue at the printer interrupt service routine (ISR) while this routine is still executing at t = 15 a communication interrupt occurs.

Q4= Solve each of the following.
The hypothetical machine of has two I/O instruction (See Fig 01)

011 = load AC from I/O
011 = Store AC to I/O

In these cases the 12-bit address identifie a particular I/O device. Show the program execution (using the format of fig 3.5) for the following program.

load AC from device 5.

Add · contents of memory location 940
Store AC to device 6
Aold contents of memory location
Assume that the next value retrived
from device 5 is 3 & that location
940 contains a value of 2.
Memory (contents in hex): 300: 3005; 301:
5940; 302: 7006 Step 1: 3005 → IR; Step 2: 3
→ AC Step 3: 5940 → IR; Step 4: 3+2=5 → AC
Step 5: 7006 → IR: Step 6: AC → Device 6

B:- The program execution of fig 02 is described in the text using six steps. Expand this discription to show the use of the MAR & MBR?

The pc contain 300, the address of the first instruction. This value is loaded into the MAR. b. The value in location 300 (which is the instruction with the value 1940 in hexadecimal) is loaded into the MBR & the PC is incremented. The two

Steps can be done in parallel c. The value in the MBR is loaded into the IR.

2 The address portion of the IR (940) is loaded into the MAR. b. The value in location 940 is loaded into the MBR. c. The value in the MBR is loaded into the AC.

3 The value in the PC (301) is loaded into the MAR. b. The value in location 301 (which is the instruction with the value 5941) is loaded into the MBR. & PC is increamented c. The value in the MBR & the PC is increamented c. The value in the MBR is loaded into the IR.

4 The address portion of IR (941) is loaded into the MAR{B}. The value in location 941 is loaded into MBR. C. The old value of the AC & the value of location MBR are added & the result is stored in the AC.

5:- The value in the PC (302) is loaded into the MAR. b. The value in location 302 (which is the instruction with the value 2941) is loaded into the MBR & the PC is incremented C. The value in the MBR is loaded into the IR.

6:- The address portion of the IR (941) is loaded into MAR. b. The value in the AC is loaded into MBR C The value in the MBR is stored in location 941.

C: Consider a hypothetical 32-bit microprocessor having 32-bit instruction composed of two fields: the first byte contain the opcode & the remainder the immediate operand or an operand address.

a: what is the maximum directly addressable memory capacity (in bytes)?

b: Discuss the impact on the system speed if the microprocessor bus has:

1 32 bit local address bus & 16 bit local data bus or

2:- 16 bit local address bus & a 16 bit local data bus.

C:- How many bits are needed for the program counter & the instruction register?

ANS:

A: $2^{24} = 16$ MBytes

b:-(1) if the address bus is 32 bits the whole addressed can be transfered at once & decoded in the memory However, because the data bus is only 16bits, it will teruire 2 cycle to fetch a 32-bit instruction or opr. and.

(2): The 16 bit of the address placed on the address bus can't access the whole memory thus a more complex memory interface control is needed to latch the first part of the address & then the second part.

C: the program counter must be at least 24bits. Typically a 32-bit microprocessor will have a 32 bit external address bus & a 32 bit program counter. unless on chip segement register are used that may work with a smaller

·program counter· if the instruction register is to contain the whole instruction it will have to be 32-bits long. if it will contain only the op code (called the op code registers) then it will have to be 8 bits long

D:- consider a 32-bit microprocessor with a 16 bit external data bus, drive by an 8-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate (bytes/sec) across the bus that this microprocessor can sustain? To increase its performance, would it be better to make its external data bus 32 bits or double the external clock frequency supplied to the microprocessor? State any other assumption you make & explain.
Hint: determine the number of bytes that can be transferred per bus cycle.

ANS:-

Clock cycle =

1 ÷ 125 NS 8 MHz Bus cycle = 4 x 125 NS = 500 NS

2 bytes transferred every 500 NS; thus transfer rate.

* 4 MBytes/Sec:-

Doubling the frequency may mean adopting a new manufacturing technology (assuming each instruction will have the same number of clock cycles) doubling the external data bus means wider (maybe newer) on chip data bus drivers (/caches & modification to the bus control logic. in first case, the speed of the memory chips will also need to double (roughly) not to slow down the microprocessor; in the second case the "wordlength" of the memory will have to double to be able to send/receive 32-bit quantities.

Q:- consider ~~a 32~~ two microprocessor having 8 & 16 bit wide external

data buses respectively. The two processor are identical otherwise & their bus cycle take just as long.

A:- Suppose all instructions & operands are two bytes long. By what factor do the maximum data transfer rate differ?

b:- Repeat if half of the operands & instructions are one byte long.

ANS: Dusing a single bus cycle, the 8 8 bit microprocess tranfer one byte while the 16 bit microprocessor transfers two bytes. The 16 bit microprocessor has twice the data transfer rate

b:- Suppose we do 100 transfers of operands & instructions of which 50 are one byte long & 50 are two bytes long. The 8 bit microprocessor takes $50 + (2 \times 16 - 50) = 150$ bus cycle for the tranfer The 16-bit microprocessor requires $50 + 50 = 100$ bus cycle. Thus the data transfer rate differ by a factor 1.5.

F:- The intel 8086 is a 16-bit processor similar in many ways to the 8-bit 8088. The 8086 uses a 16-bit bus that can transfer 2-bytes at a time, provided that then lower order byte has an even address, However, the 8086 allow both even & odd aligned word operands. if an odd aligned word is referenced, two memory cycle, each consisting of four bus cycle are required to transfer the word. Consider an instruction on the 8086 that involves two 16-bit operands. How long does it take to fetch the operands? Give the range of possible answer. Assume a clocking rate of 4MHz & no wait states.

ANS:- A bus cycle take 0.25 us So a memory cycle take 1 us. if both operand are

even aligned it take 2 μs to fetch the two operands. if one is odd-aligned, the time required is 3 μs. if both are odd-aligned the time required is 4 μs.

Q:- Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that on average 20% the operands & instruction are 32 bits long 40% are 16 bit long & 40% are only 8 bits long. Calculate the improvement acheived when fetching instruction & operands with the 32-bit microprocessor.

ANS:- Consider a mix of 100 instruction & operands. on average they consist of 20% 32 bit items, 40% 16-bit items, & 40% 8-bit items. The number of bus cycle required for the 16-bit microprocessor is $(2 \times 20) + 40$

+ 40 = 120. For the 32 bit microprocessor, the number required is 100. This amounts to an improvement of 20/120 or about 17%.