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Subject # Electronic device & circuit

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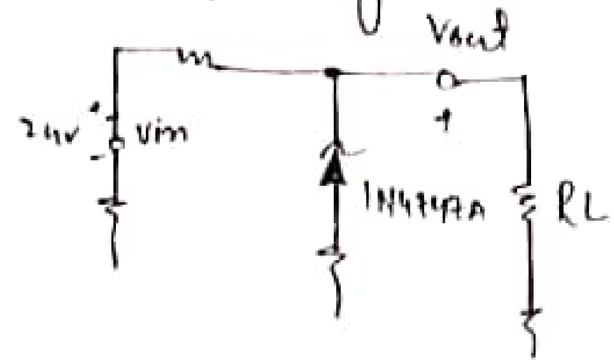
Deparment # B(EE)

Semester # 8th

Q1: The IN4747A zener used in the regulated circuit of figure 1 is a 20v diode determine the following.



Answer:

from the datasheet IN4747A $V_Z = \cancel{20}$ 15 $I_Z = 12.5$ and $Z_Z = 22\Omega$ $I_{ZK} = 0.25$

(a) for I_{ZK}:

$V_{out} = V_Z - \Delta I_Z Z_Z$

$= 20 - (I_Z - I_{ZK}) Z_Z$

$= 20 - (12.25mA)(22\Omega) = \boxed{19.7305V}$

$= ~~15V - (0.01225)(22)~~$

$= \boxed{~~14.7305V~~}$

Calculating zener Max current the maximum Power dissipation is 1w

$I_{ZM} = \frac{PD(Max)}{V_Z} = \frac{1w}{20} = ~~0.06667A~~$ 0.05

$I_{ZM} = \boxed{~~66.7mA~~}$ $\boxed{50mA}$

For I_{ZM}:

$V_{out} = V_Z + \Delta I_Z Z_Z$

$= 20 + \Delta I_Z Z_Z$

$= 20V + (I_{zm} - I_z)Z_z$

$= 20V + (0.0542)(20) =$ **21.1924V**

$= 20 + 7.7~~...~~ =$ **~~16.1924V~~**

b) Calculate value of R for max zener current that occurs when there is no load

$R = \frac{V_{in} - V_Z(max)}{I_T}$ or $\frac{V_{in} - V_{out}}{I_{zm}}$

$I_L = 0$
$I_z =$
$I_{zm} = I_T$

$= \frac{24V - 21.1924V}{I_{zm}}$ (~~16.1924V~~) $= \frac{24V - 21.1924V}{50mA} = 2.8076$ ~~7.8076~~ $= 1$~~4.5313~~ $= 56.152\Omega$ ~~...mA~~

R = 1~~2~~0Ω $R \simeq 60\Omega$

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Q2:

Determine I_B, I_C, I_E, V_{BE}, V_{CE}, and V_{CB} in the circuit.

Answer:

we know that $V_{BE} \cong 0.7V$ Calculate the base, collector and emitter currents as follows.

$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5V - 0.7V}{3.9k\Omega} =$ **1102.564µA**

$I_C = \beta_{DC} I_B = (150)(1102.564\mu A) =$ **165.384 mA**

$IE = IC + IB = 165.384 mA + 1102.564 mA$

$= \boxed{1267.948 mA}$

⇒ Solve for VCE and VCB.

$VCE = VCC - ICRC = 15V - (165.384 mA)(180 \Omega) = 15 - (0.0655)(180)$

$= 15 - (77.79) = \boxed{3.21V}$

$VCB = VCE - VBE =$

$3.21 - 0.7 = \boxed{11.79V}$

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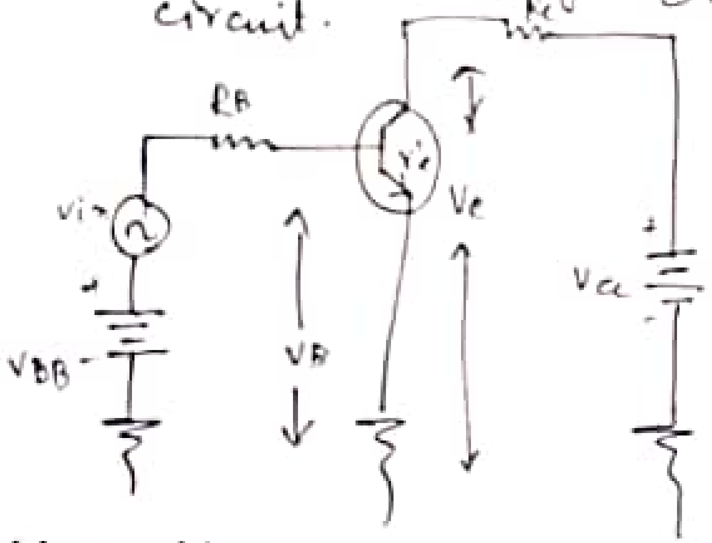
Q3:-

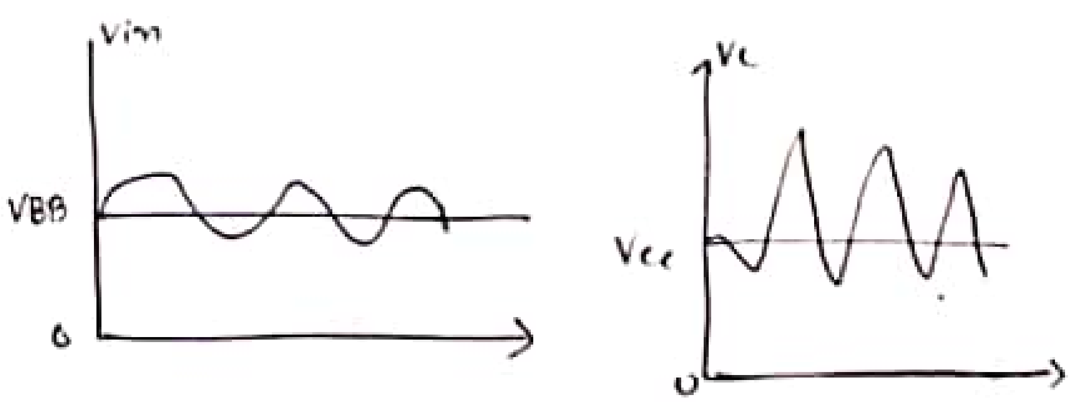
⇒ The BJT AS AN AMPLIFIER:

Amplification of a relatively small ac voltage voltage can be had by placing the ac signal source in the base circuit.

Recall that change in the base current circuit causes large change in collector current circuit.



(a) circuit with ac input voltage Vin and dc bias voltage superimposed.



(b) Waveforms.

The ac emitter current: $I_e \approx I_c \approx V_b / r'_e$

The ac collector voltage: $V_c = I_c R_c$

Since $I_c \approx I_e$ the ac collectorvoltage: $V_c \approx I_e R_c$

The ration of V_c to V_b is the ac voltage gain:

$A_v = V_c / V_b$

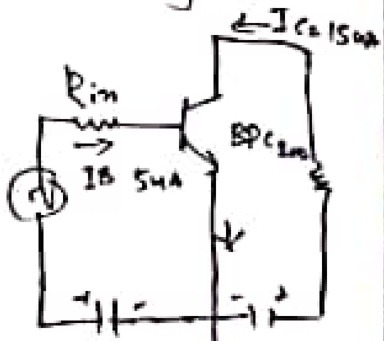
Substisting $I_c R_c$ for V_c and $I_e r'_e$ for V_b: $A_v =$
$V_c / V_b = I_c R_c / I_e r'_e$

⇒ The I_c terms cancel: $A_v = R_c / r'_e$

for using BJT as an amlifener we need to set them in Active region because BJT working as an amlifier when use is active region.

⇒ Transistor has three Bases configuration for using it in Amplification mode.

Common Base: Voltage gain no current
common emitter: Both gain
" Collector: current gain no voltage



So this is comon emitter cofiguration of transistor which has both transfer which has both voltage & current amplification.

$I_C = B \cdot I_B = 200 + 5uA$

$I_C = 200 + 5uA = 200000 5uA$

$I_E = I_C + I_B = 200 \cdot 0000\ 5uA + 15uA =$ $\boxed{200.002A}$

Q4:

Answer:

Trainsistor Full ON (ON)

Transistor Full OFF (OFF)

Input and base are at OV (OFF)

Colloector Current $I_C = 0$ (OFF)

$V_{CE} = V_{CC}$ (OFF)

BE Junction is reversers bias (OFF)

BC Junction is forward biase (OFF)

Maximum of saturation current I_C flow (ON)

BE Junction is forward bias (ON)

BC Junction is forward bias (ON)

$V_{CE} = 0V$ (ON)

BE Juntion is less then 0.7V (OFF)

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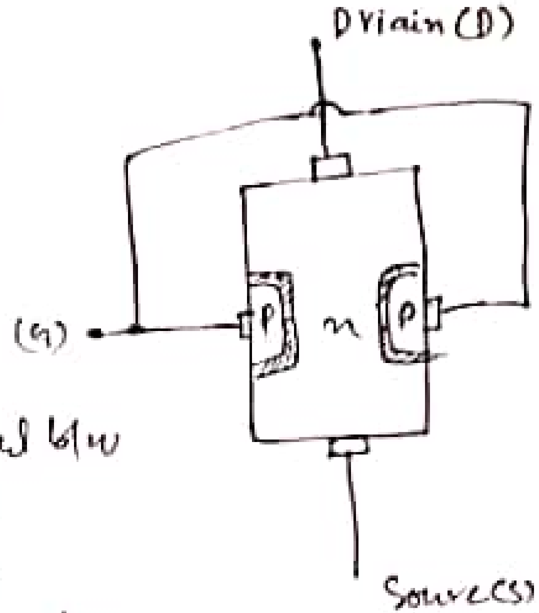
Q5:

Answer:-

→ N-Channel JFET:-



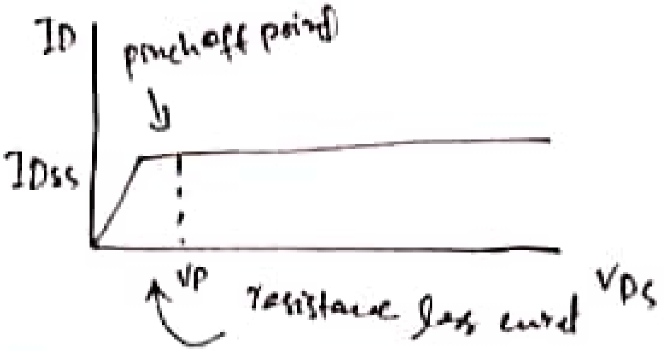
* Two p-type material
* one n " "
* So there is n-channel b/w two p-type material.
* Three terminal device.
* There are two pn junction so we have two deplation region.
* If width of depeation reginon is increased the n-channel will get narrow and flow of e. towards drain will be decrased.
* Flow of e is controlled by the Gate
* The depletion region is controlled by VGS- or o/p current is " by VGS.
* It is a voltage controlled device.

→ JFET as Constant current Source:-

* can be used as cc source when

$I_D = I_{DSS}$

and $V_{DS} > V_P$ and $V_{DS} < V_{DSmax}$ V_{DSmax} = breaking voltage

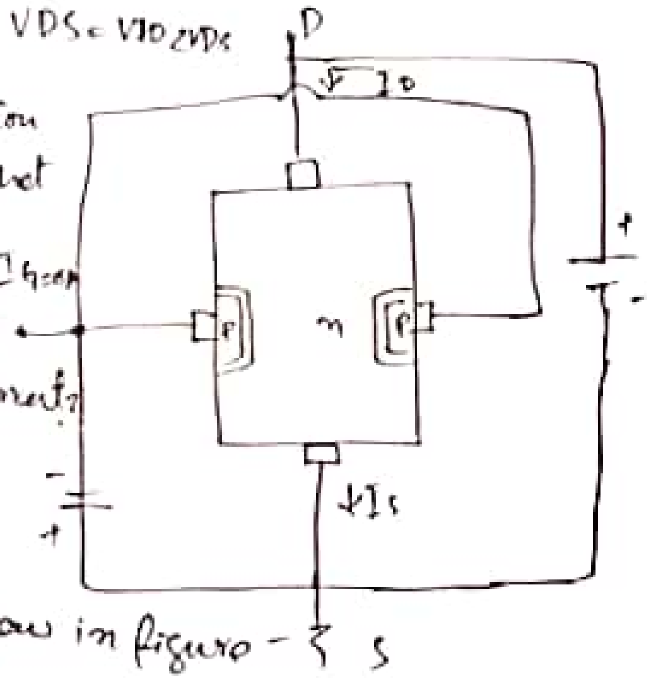


IDss :- is max drain current when VGS=0V and VDS > |Vp| Vp = pinch volt

⇒ Working of JFET:-

case 2: VGS<0V and VDS = VDD<VDS

Goal: it to obtain Saturation at lower value of VDS, so that why here VDD < VDD



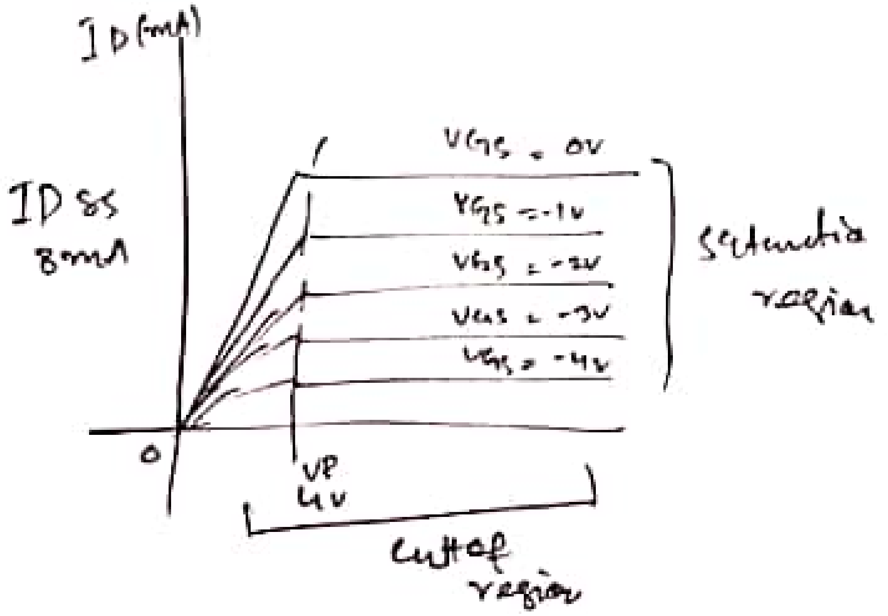
* let use how do we get the ID Saturation current?
* To make VGS more negative use do battery conecting as show in figure - 3

* Because of these connation the deplation region will change The current ID will flow and the current IG will be zero. because of reverse biased PN Junction.
* Let suppose the VGS is -1V. Beacuse of It is polarity the VGS = -1V
* The width of DR will increase because P-type is connection to lower potential and n-type is connected to higher Pontential

* width will increase more at top than bottom
* After sometime the DR at top get too much closer and reaches pinch off condition
* The pinch off voltage in this case is lowe because gate is at negatively biased
* If we increase VDS more the ID will remain same.

⇒ output or Drain Characteristic of JFET (n-channel)

* ID vs VDS
  o/p o/p
  Current voltage
  we obtain both
* For different VGS value
* The centraling voltage in VGS
* Increase of n-channel → VG<0V
  " " → VGS>0V



case 1:-

$V_{GS} = 0V$

$V_{DS} > |V_P|$ ..

$I_{DSS} = 8mA$

$V_P = -4V$

n-chan → +ve ⎤
P-chan → -ve ⎦ RB

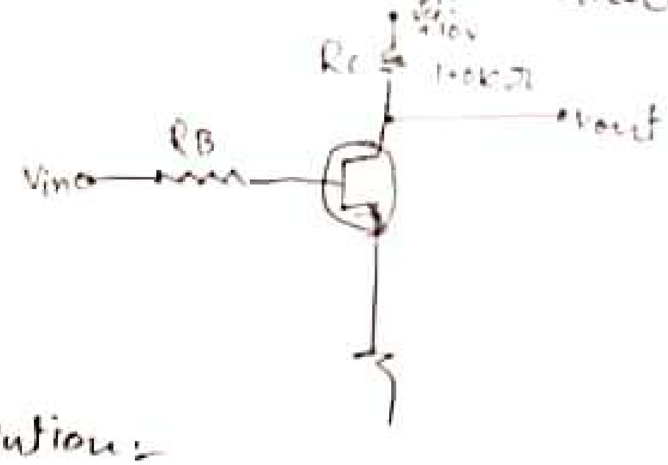
⇒ case 2: $V_{GS} = -1V$

⇒ case 3: $V_{GS} = -2V$

⇒ case 4: $V_{GS} = -3V$

⇒ case 5: $V_{GS} = -4V$

Q6: For the transistor circuit given



Solution:-

(a) $V_{CE} = ?$ $V_{in} = 0V$

when $V_{in} = 0V$ So transmitter is cutoff mode

$V_{CE} = V_{CC} = 10V$

(b) V_{in} $I_B = ?$ $\beta_{DC} = 125$

$V_{CE(sat)} = 0.4V$

$$I_C(sat) = \frac{V_{CC}}{R_C} = \frac{10V}{1.0k\Omega} = 10mA$$

$$I_B = (Min) = \frac{I_C(sat)}{B_{DC}} = \frac{10mA}{125}$$

$$I_B(min) = \boxed{0.08\,MA}$$