Department of Electrical Engineering
Assignment
Date: 20/04/2020

Course Details

Course Title:	**VLSI Technology**	**Module:**	**6th**
Instructor:	**Engr. Zulqarnian**	**Total Marks:**	

Student Details

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Part A (Objective Type)

1. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance??
   a. Static dissipation
   b. Dynamic dissipation
   c. Both a and b
   d. None of the above.

2. Which type of MOSFETS Exhibits no current at zero gate voltage?
   a. Depletion MOSFET
   b. Enhancement MOSFET
   c. Both a and b
   d. None of the above

3. CMOS circuits are constructed in such a way that all PMOS transistors must have either an input from the voltage source or from another
   a. PMOS transistor
   b. NMOS transistor
   c. CMOS transistor
   d. BJT transistor

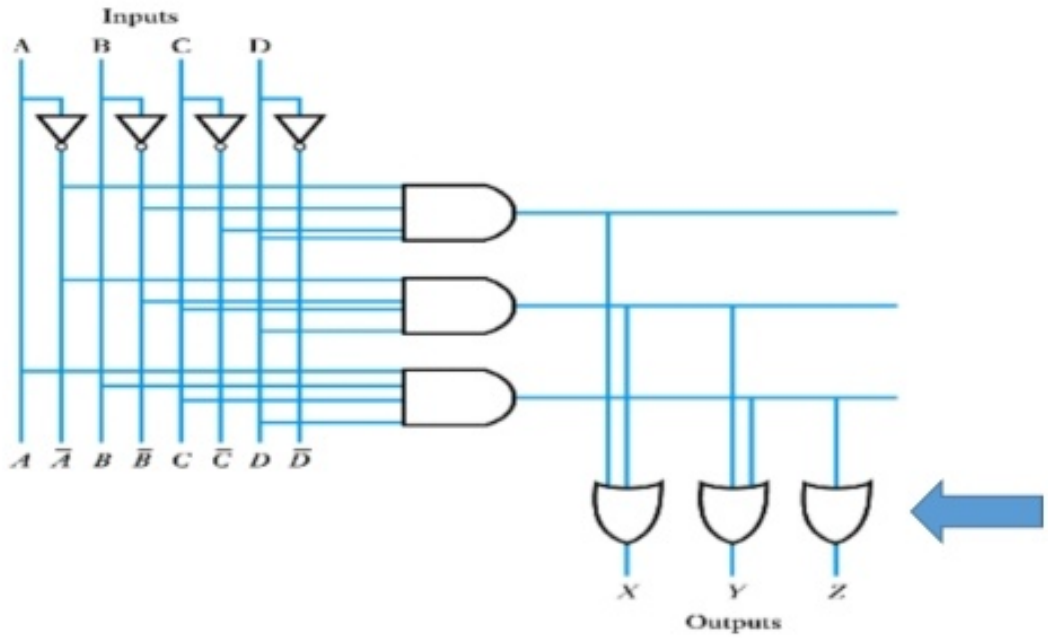
4. Delay which is equal to the time taken by a gate output transition to 0, from another value 1, x, or z is
   a. Rise delay
   b. Fall delay
   c. Turn-off delay
   d. Turn-on delay

5. Which type of simulation model is used to check the timing performance of a design?
   a. Transistor level
   b. <u>Gate level</u>
   c. Behavioral
   d. Switch level
   e. None of these

6. Which of the following statements is incorrect
   a. Some PLDs are programmed using electrically operated switches.
   b. <u>Some PLDs are programmed using mechanical switches</u>

Fill in the Blanks

7. In MOS devices, the current at any instant of time is **<u>Constant & independent</u>** of the voltage across their terminals.
8. For complex gate design in CMOS, OR function needs to be implemented by **<u>Parallel</u>** connections of MOS
9. In the following PLA, which output implements the logic function ABCD??



Output logic function of ABCD is **<u>Z.</u>**

10. The term VLSI means a device containing between **<u>Thousand</u>** and **<u>Million</u>** transistors.

Q1:- In low power VLSI design clock gating technique will reduce power all time or it depends upon the input date? In any chance the computation power may increase?

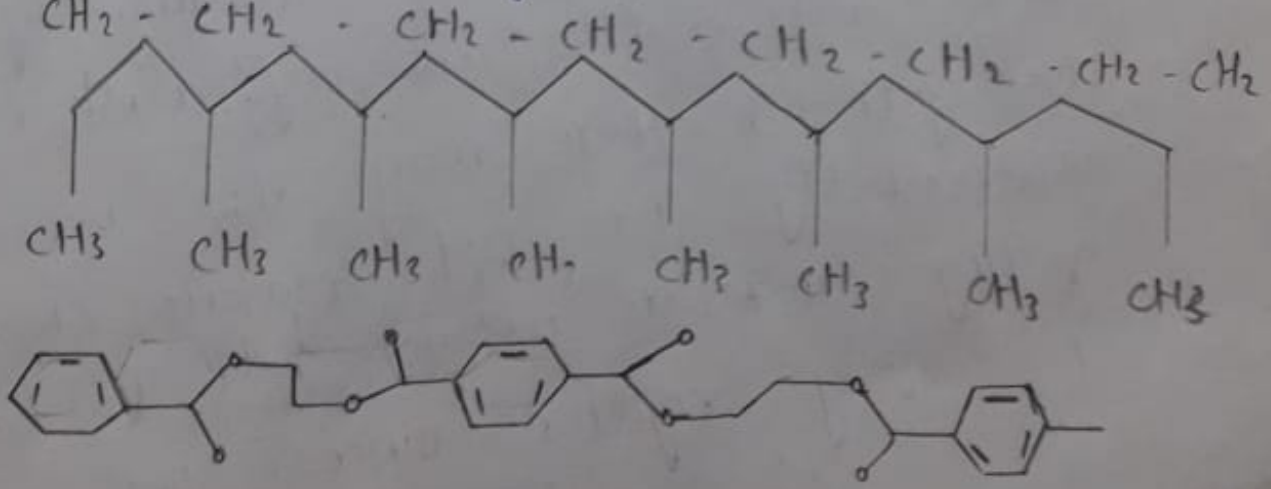
Ans:- Using this clock-gating technique the flip-flop clock only when the output has to change. Clearly this mean that the flop will clock less this circuit than in the previous one.

In reality when this is done via the synthesis tool rather than just an "and" gate a latch. Integrated cell in the libbrys is used with the and to prevent glitch issues when the timing of the clock and enable are different (clock-tree synthesis) there may also be added observability tol Dft reasons clearly a gating structure would not be applied to every register since the cost in

Power it the gating would etceed the saving on a flop.

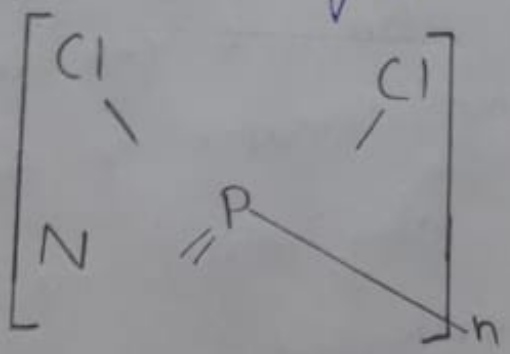
Q 2 B):- While fabrication .t NMOS or PMOS we usually use inorganic Polymer. If we use organic Polymers instead .t inorganic Polymer what will happen!

Ans:- Organic polymers are polyme material that essentially contain carbon atoms in the backbone. Therfore, there are only carbon covalent bond in these. These polymers only from organic monomers molecules. Most of the times, these Polymers are environmental friendly since these are biodegrdble.



Furthermore these are two major forms of organic polymers such as natural and synthetic polymers common example of important organic polymers include polysachoride proteins, polynucleotides (DNA and RNA) etc.

Inorganic polymers are polymer material that have no carbon atoms in the backbone. However most of these are some organic regions as well these materiable are highly branched sturctures and have chemical element other than carbon ex: sulfer nitrogen.



Moreover these polymers are not environmentlly friendly because they are not biodegradbly. Some common example include polydimethesiltane (sillicon rubber) polyphosphazels etc.

Q2 a) If we want to design an IC and I want that each every transistor used in this IC should be optimized individully with less time. How it will be possible?

Ans:- A transistor is a semiconductor device used to amplify or switch electronic signals and electrical power. It is composed of semiconductor material usually with at least three terminals for connection an external circuit. A voltage of circuit applied to one pair of the transistor terminal control the current through another pair of terminal. Because the control (output) power can be higher than the controlling (input) power a transistor can simplify a signal. Today some transistor are packed inallvidually but many more are found embedded in integrated circuit.

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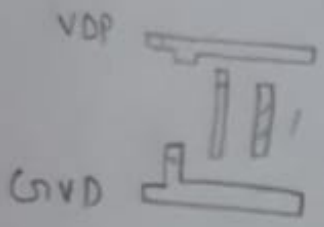
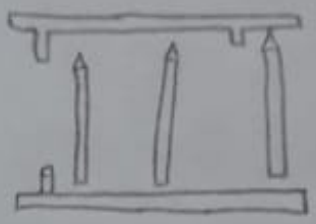
Q3:- Draw a stick diagram of a layout using that variable ordering F = ACD + ABD.

Ans:- Stick Diagrams.

Stick diagrams help plan l-put quickly

- Need not be to scale
- Draw with color pencil or dry-erase marker.





Wiring Tracks

-> A wiring track is the speed required for a wire 4 λ width 4λ spacing from neighbor = 8 λ pitch

-> Transistor also consume one ustoy track

☆ Well spacing

Well must surround transistor by 6λ ~~flavors~~

- implies 12 λ between opposite transistor flavors.

- Leaves room for one wire track

* Area Estimation

Estimation area by counting wiring tracks.

Multiple by 8 to express in λ.