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Submitted to Sir Amin

Subject Computer Architecture

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Answer the Questions.

A Discuss the two approaches for dealing with multiple interupts?

Ans The first is to double interupts while an interupt is being processed. A disabled interupt simply means that the processor can & will ignore the interupt request signal.

* The drawback to the preceding approach is that it doesn't take into account relative priority or time critical needs.

2. A second aproach is to define priorities for interupts & to allow an interupts of higher priority to cause a lower priority interupt hander to be itsely interupted.

b. Discuss the types of exchanges that are needed by indicating the major forms of input & output for processor, memory & I/O modules?

Ans Following are the types.

* Memory to processor:-
The processor read that instruction or a unit of data from memory.

* Processor to memory:-
The processor write a unit of data to memory.

* I/o to processor:-
The processor read data from I/o device via an I/o module.
* Processor to I/o:-
The processor send data to the I/o data.
* I/o to or from memory:-
From these two loao cases an I/o modules is allow to exchange data directly with memory, without going through the processor, using direct memory access.

C) Discuss the quickpath interconnect (QPI) protocol layers?

Ans QPI protocol layer:-
In this layer the packet is defined as the unit of transfer. one key function performed at this level is cache coherency protocol, which deals with making sure that main memory values held in multiple cache are consistent. A typical data packet payload is a block of data being sent to or from a cache.

d) Discuss the physical & logical architecture of PCIe in detail?

* Physical & logical architecture of PCIe:-

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* A root complex device, also refered to as a chipset or a host bridge connects the processor & memory subsystem to the PCI express switch fabric comprising one or more PCIe & fabric switch devices.
* PCIe links from the chipset may attach to the following kind of devices that implement PCIe.
* **Switch:-**
  The switch manages multiple PCIe streams.
* **PCIe end point:-**
  An I/O device or controller that implement PCIe such as a Gigabit ethernet switch, a graphics or videos controller.
* **Legacy endpoint:-**
  Legacy endpoint category is intended for existing design that have been migrated to pci & its allow legacy behaviour such as use I/O space & locked transaction.
* **Pcie /Pci bridge:-**
  Allows order PCI device to be connected to PCIe based system.

Write Short note on each of the following.

A. **Instruction cycle:-**
  The processing required for a

single instruction is called an instruction cycle. Using the simplified two step description given previously the instruction cycle is depicted. The two steps are refered to as the fetch cycle & the execute cycle. Program execution halts only if the machine is turned off. Some sorat of unrecoverable error occurs, or a program instruction that halts the computer is encountered.

B. Instruction cycle state diagram:

* Instruction cycle address calculation (IAC)
  Determine the address of the next instruction to be executed.
* Instruction fetch (If):-
  Read instruction from its memory location into the processor.
* Instruction operation decoding:-
  Analyze instruction to determine the type of operation to be performed & operand(s) to be used.
* Operand address calculation (OAC):-
  If the operation involve reference to an operand in memory or available via I/O then determine the address of the operand.
* Operand fetch (of):-
  Fetch the operand from memory

or read it in form I/O.

* Data operation:-
Perform the operation indicated in the instruction.

* Operand stor (OS):-
Write the result into memory or out to I/O.

C) Causes of interput:-
Its generated by same conditon that occur as a result of an instruction execution such as arthimetic overflow, division by zero attempt to execute an illelegal machine instruction, or reference outside a User's allowed memory space.

Timer:-
Its generated by a timer within a processor. This allows the operating system to perform certain function on a regular basis.

I/O:-
Its generated by an I/O controller to signal normal completion of an operation request service from the processor, or to signal a variety of error condition.

D) Bus interconnection scheme:-
The most common computer interconnection structure are based on

the use of one or more system buses.

Data lines:-

The data lines provide a path for interconnection structure are based on the use of one or more system buses.

Data lines:

The data lines provide a path for moving data among system module. These lines collectively are called the data bus.

Address lines:

The address lines are used to designate the source of destination of the data on the data bus.

Control lines:

Control lines are used to control the access to & the used of the data & address lines. Because the address & the data lines are stored by all components.

Differentiate each of the following:

A - Programming in hardware & programming in software.

Programming in hardware:

The program is in the form of hardware & term a hardware program suppose we construct a general purpose configuration

of arithmetic & logic function. This set of hardware will perform various function on data depending on control signals applied to the hardware. In original case of customize Hardware the system accept data & produce results.

Programing in software:-

The new method of programming which is a seqvence of codes or instruction is called software. In this method programming is much easier, instead of rewiring the hardware for each new seqvence of code each code is in effect an instruction & part of the hardware interupts each instruction & generates control signals.

B) Program flow of control without interupt & with interupt.

Ans In the interupt cycle, the processor check to see if any interupts have occured, indicated by the presence of interupt signal.

* If no interupt are pending, the processor proceed to the fetch cycle & fetches the next instruction of the current program.

c) Disabled interupt & nested interupt processing.

Ans A disabled interupt simply means that processor can & will ignore that interupt request signal if an interupt occur during this time it generally remain pending & will be checked by the processor after the processor has enabled interupts.

* A nested interupt is to allow an interupt of higher priority handler to be itself interupted. A user program begins at t = 0, At t = 10 a printer interupt user information is placed on the system stack & execution continue at the printer interupt service routine (ISR) while this routine is still executing at t = 15 a communication interupt occurs.

Q4 Solve each of the following.

The hypothetical machine of has two I/O instruction (see fig 01)

011 = Load AC from I/O

011 = Store AC to I/O

In these cases the 12-Bit address identify a particular I/O device. Show the program execution (using the format of fig 3.5) for the following program.

Load AC from device 5

Add contents of memory location 940 store Ac to device 6.

Add that the next value retrieved from device 5 is 3 & that location 940 contains a value of 2.

Ans Memory (contents in hex): 300: 3005, 301: 5940; 302; 7006 step 1: 3005 → IR; step 2: 3 → Ac step 3: 5940 → IR: step 4: 3+2=5 → Ac step 5: 7006 → IR: step 6: Ac → Device 6

B) The program execution of fig 02 is described in the text using six steps. Expand this discription to show the use of the MAR & MBR?

Ans The Pc contain 300, the address of the first instruction. This value is loaded 300 (which is the instruction with the value 1940 in hexadecimal) is loaded into the MBR & the Pc is incremented. The two steps can be done in parallelic. The value in the MBR is loaded into the IR.

2 The address portion of the IR (940) is loaded into the MBR.b. The value in location 940 is loaded into the MBR.c. The value in the MBR is loaded into the Ac.

3 The value in the pc (301) is loaded into the MAR.b. The value in location (301)

is loaded into the MBR & Pc is incremented c. The value in the MBR & the Pc is incremented c. The value in the MBR is loaded into the IR (941).

4) The address portion of IR (941) is loaded into the MAR (B). The value of the ac & the value of location MBR are added & the result is stored in the AC.

5 The value in the Pc (302) is loaded into the MAR. b. The value in location 302 is loaded into the MBR & the Pc is incremented c. The value in the MBR is loaded into the IR.

6 The address portion of the IR (941) is loaded into MAR. b. The value in the AC is loaded into MBR c. The value in the MBR is stored in location 941.

c Consider a hypothetical 32-bit microprocessor having 32-bit instruction composed of two fields the first byte contain the opcode & the remainder the immadidte operand or an operand address.

a. What is maximum directly addressable memory capacity (in bytes)?

b. Discuss the impact on the systen speed if the microprocessor bus has.

1 32 bit local address bus & 16 bit local data bus or.

2) It data bit local address bus & a 16 bit local data bus.

c How many bits are needed for the program counter & the instruction register.

Ans 2^{24} = 16 M Bytes

b (1) If the address bus is 32 bits the whole addressed can be transfered at once and decoded in the memory. However, because the data bus is only 16 bits, it will require 2 cycle to fetch a 32-bit instruction or opreand.

2) The 16 Bit of the address placed on the address bus can't access the whole memory thus a more complex memory interface control is needed to latch the first part the address & then the second part.

C The program counter must be at least 24 bits. Typically a 32-bit microprocessor will have a 32 bit external address bus & a 32 bit program counter. Unless on chip segment register are used that may work with a smaller program counter. If the instruction it will have to be 32-bits long. If it will contain only the op code (called the op code registers) then it will have to be 8 bits long.

D) Consider a 32-bit microprocessor with a 16 bit external data bus, drive by an 8-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate accross the bus that this microprocessor can sustain? To increase its performance, would it be better to make its external data bus 32 bits or double the external clock frequency supplied to the microprocessor State any other assumption you make & explain.

Ans Clock cycle

1= 125ns 8 MHZ Bus Cycle = 4x125ns = 500ns
2 bytes transferred every 500ns, thus transfer rate.

* 4m Bytes/sec

Doubling the frequency may mean adepting a new manufacturing technology doubling the external data bus means wider (maybe newer) on chip data bus control logic In first case, the speed of the memory chips will also need to double not to slow down the microprocessor in the second case the 'word length' of the memory will have to double to be the memory will have to double to be able to send/recive 32-bit quantities.

e) Consider two microprocessor having 8 & 16 bit wide external data buses rapectively. The two processor are identical otherwise & their bus cycle take just as long.

A. Suppose all instructions & operands are two bytes long. By what factor do the maximum data transfer rate differ?

b. Repeat if half of the operands & instruction are one byte long.

Ans During a single bus cycle, the 8 bit microprocessor transfer one byte while the 16 bit microprocessor transfer two bytes. The 16 bit microprocessor transfer two bytes. The 16 bit microprocessor has twice the data transfer rate.

b. Suppose we do 100 transfers of operands & instructions of the 50 are one Byte long & 50 are two bytes long. The 8 bit microprocessor takes $50 + (2 \times 16 - 50) = 150$ bus cycle for the transfer. The 16-bit microprocessor requires $50 + 50 = 100$ bus cycle. Thus the data transfer rate differ by a factor 1.5.

f) The intel 8086 is a 16-bit processor similar in many ways to the 8-bit 8088. The 8088 uses a 16-bit bus that can transfer 2-bytes at a time.

Provided that then lower order byte has an even address, However the 8086 allow both even & odd aligned word is referenced, two memory cycle each consisting of four bus cycle are required to transfer the word. Consider an instruction on the 8086 that involves two 16-bit operands. How long does it it take to fetch the operand. Give the range of possible answer. Assome a clocking rate of 4 MHZ & no wait states.

Ans A bus cycle take 0.25 us so a memory cycle take 1 us - If both operand are even aligned, it take 2 us to fetch the two operands, If one is odd aligned the time required is 3 us. If both are odd - aligned the time required is 4 us.

Q Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that an average 20 % the operands & instruction are 32 bits long 40 % are 16 bit long. Calculate the improvement achieved when fetching instruction & operands with the 32-bit microprossesor.

Ans Consider a mix of 100 instruction & operands. on average they consist

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of 20% 32 bit items, 40% 16-bit items, & 40% 8-bit items. The number of bus cycle required for the 16-bit microprocessor is (2x20)+40+40 = 120. For the 32 bit microprocessor, the number required is 100. This amount to an improvement of 20/120 or about 17%.